

Comparison of two Pentium MCMs implemented in different Technologies

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Abstract

Two Pentium Multi-Chip Modules (MCM) containing a Pentium Processor, part of the Intel Chipset and 512kBytes 2nd level cache are compared in this paper. Since these two modules are targeted at different markets, they are implemented in quite different technologies. Both modules were developed at the Electronics Laboratory of the ETH Zürich. One module is built on a four layer MCM-D substrate and packaged in a Plastic Stud Grid Array Package (PSGA), developed by IMEC. The complete module is treated like a standard SMT component. The second module is a mix of SMT and Chip-on-Board (COB) technology. Therefore the substrate is an eight layer laminate with laser-drilled microvias, which is populated on both sides. The second level interconnection is provided by two SMT connectors on two sides of the module. The comparison of these two MCMs should reveal the impact of a chosen target market on partitioning and technology.

Key words: MCM-D, COB, Die, Pentium Module

1 Introduction

MCM design is not a straight forward process, since the packaging strategy, such as the selection of bonding and substrate, has to meet the demands of addressed market. Partitioning as well as build-up technology is crucial for the success of the design. In the following, we want to examine two implementations of nearly the same system in different technologies. In an earlier paper [2] an exhaustive examination of all possible realisations is done. The focus in this paper is on the impact of the target market on decisions regarding technology and partitioning. In the following section a short description of the system and the two implementations is given. The third section explains why different tech-

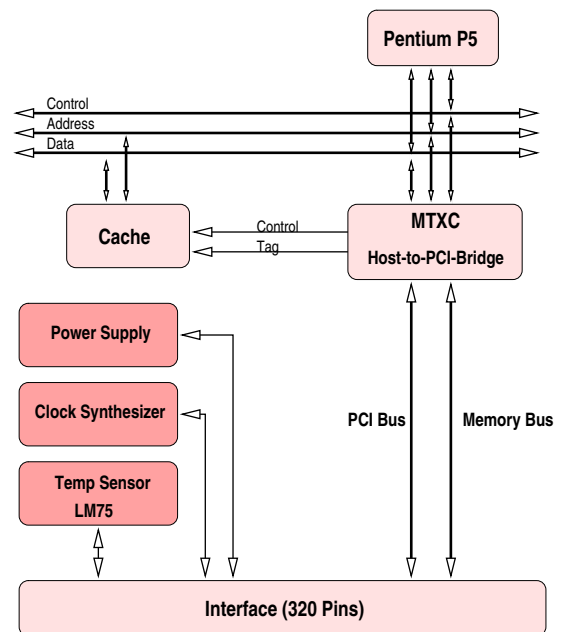


Figure 1: Architecture of the MCMs

nologies are used for the two modules. The next section compares the two modules in various aspects (mechanical, thermal and cost). Finally the present status and an outlook to further activities is given.

2 System overview

Both designs are based on the idea of encapsulating the core of a pentium system with its wide high speed host bus on a high density substrate. This results in a substantial reduction of external connections. Both modules have a standard interface to PCI- and Memory bus. The system realized on the two modules is basically the same: Pentium Processor, parts of the

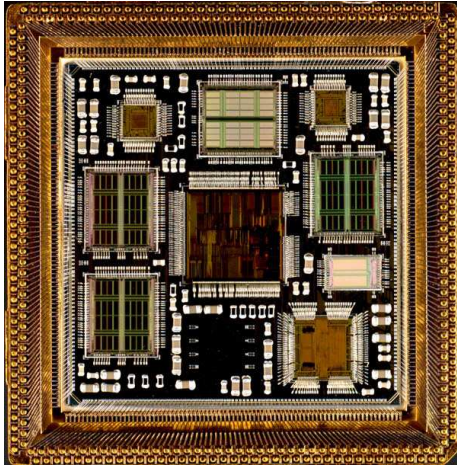


Figure 2: Pentium MCM

chipset (Host-to-PCI-Bridge) and 512 kByte 2^{nd} level cache (figure 1). Due to the different target applications, the SMART-P5 module has added functionality. This renders the interface even more universal, but excludes a highest density MCM-D solution. The additional features of the SMART-P5 module are a 2.45V switched voltage supply, a temperature sensor and a clock synthesizer. The designer has to be aware of the implications of the chosen partitioning, because decisions taken at an early stage of the project (partitioning) can limit the available technologies. E.g. the voltage supply on the SMART-P5 module cannot easily be integrated on an MCM-D substrate, because of its many and large components.

3 Technologies of the two MCMs

In order to find the appropriate choice for bonding option, substrate type, cross section cooling and test strategy a feasibility analysis has to be done. The combination of technologies has to be chosen carefully regarding the key attributes like mechanical specification (form factor and height), electrical specification (signal integrity), thermal aspects and economical specifications (yield and cost). For both designs aluminum wire bonding was selected due to good availability and well adjusted processes of the technology.

Since for the first module minimal size and overall height was imperative, the module is based on a MCM-D Thin-Film on Silicon technology (figure 2).

Only this type of the substrate allows enough integration to reach the desired form factor of 32mm·32mm for the substrate. With the chosen design rules (table 1), all ICs can be assembled as bare dies and can be wire bonded with 25 μm aluminum wire. The substrate manufacturing and assembly was

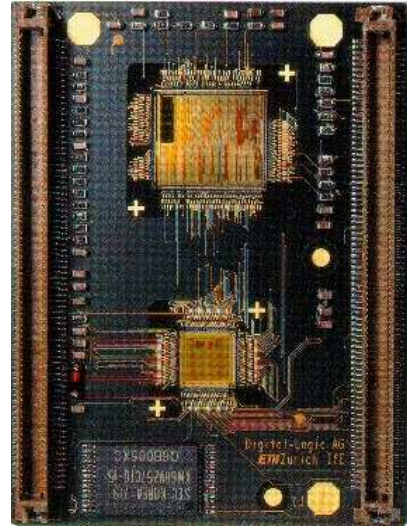


Figure 3: SMART-P5 Module, Die Side

done by companies within EURORACTICE MCM Service¹. This selection of technology and manufacturers results in the smallest Pentium MCM at reasonable cost. The requirements for the SMART-P5 module (figure 3) were slightly different. Designed for the use in embedded systems, the SMART-P5 module should enable the user to design a complete Pentium system with as little external design effort as possible and at low cost. Furthermore, the module should be removable in field. The system has to fit on a PC/104 card, so small size was a matter, but not highest priority. Therefore only the most space-wasting components (Pentium, System Controller) are mounted directly onto the substrate (Chip-on-board). The rest is mounted as SMT single chip packages. Though the SRAMs of the cache are quite big, they are populated as packaged devices (figure 4). This improves yield, which minimizes cost of the module. This mix of mounting technologies does not allow the highest density possible, but it represents a solution at much lower cost than a MCM-D. The substrate requirements are relaxed and can therefore be fulfilled by the lower cost MCM-L solution, so for the SMART-P5 module the choice of the substrate technology was obvious. As the required design rules for the substrate were close to the limits of laminate technology, many discussions with the substrate manufactures and assembly houses were necessary to ensure a later series production. This also includes the evaluation of having bonding with soldering attachment on one side of the substrate. The final

¹EURORACTICE MCM Service was established by the EC to stimulate state-of-the-art microelectronics technologies by European industry.

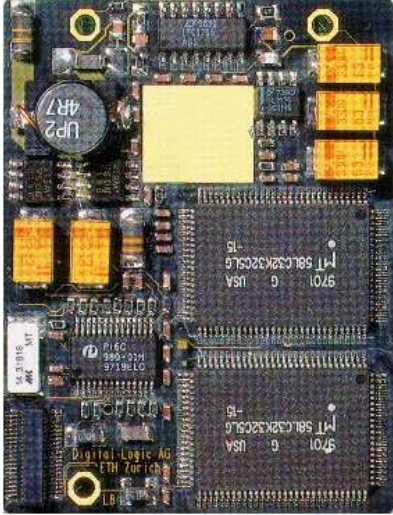


Figure 4: SMART-P5 Module, SMT side

decisions were then taken after a cost evaluation. The substrate is a PCB type laminate with laser-drilled microvias. With the given design rules (table 1) results a eight layer board with two Surface-Built-Up (SBU) layers on each side [1].

Table 1: Substrate Characteristics of Pentium MCM

	MCM-D Module	SMART-P5
Substrate Type	Thin-Film Si	Laminate BT
Design Rules		
Via Land	50 μm	200 μm
Line Space	30 μm	50 μm
Line Width	20 μm	50 μm
#Layers	4	8

4 Comparison

Since the MCM-D module is designed for applications with small space and limited weight, such as Notebooks and PDAs, it is packaged in an PSGA (Plastic Stud Grid Array) which is a plastic package very similar to a BGA package. Therefore, it looks to the customer like a single chip package. In embedded systems a modular concept, that enables the customer to exchange a part and enhance the system, is more important than small scale. This modularity is achieved by realizing the second level interconnect as SMT connectors. As a consequence the SMART-P5 module is bigger than the Pentium MCM. But as the space underneath the module is available for the placement of SMT components (table 2), the SMART-

P5 wastes less board space than the Pentium MCM. This concept of stacking the module results in an overall height of 16mm (measured from the motherboard), which is significantly higher than the 3mm of the Pentium MCM, but tolerable in most embedded systems, since it fulfills the PC/104 specifications.

Table 2: Mechanical

Property	MCM-D Module	SMART-P5
Form Factor	43mm·43mm	45mm·59mm
Board space	43mm·43mm	2·10mm·59mm
Height	3mm	16mm
Thermal Path		2.4 K/W

For the cost comparison the material cost is left aside, as there are basically the same parts on both modules. The cost factors, where the two modules differ, are the costs for substrate and assembly. The costs for the laminated substrate is substantially lower than the cost for the smaller, but much denser MCM-D substrate. The cost for assembly can be split in costs for die placing, wire bonding, testing and packaging. As the dies on both modules are bonded with aluminum wire, there is no technology-dependant difference. The number of bonds as well as the number of dies will drive the costs, because the assembly cost follow the equation below.

$$C_{Assembly} = C_{Die} + C_{Wire} + C_{Pack} \quad (1)$$

$$C_{Die} = \#Dies \cdot C_{perDie} \quad (2)$$

$$C_{Wire} = \#Bonds \cdot C_{perBond} \quad (3)$$

The cost for die and wire bonding follows the number of dies or bonds, respectively. Regarding this, it's evident that the assembly costs of the SMART-P5 module are significantly lower. The cost for the SMT process is not included in this analysis.

Table 3: Cost Comparison

	MCM-D Module	SMART-P5 ²
Substrate Cost (relative)	1.7	1
Assembly Cost (relative)	1.8	1

To get a first impression of the influence of the yield on the overall costs of the module, we calculate the theoretical yield of the bonding process. We assume the substrate to be qualified and electrically tested. According to the assembly house, a bond of a packaged

Table 4: Yield Comparison

	MCM-D Module	SMART-P5
Number of Dies total/KGD ³	9/4	2/2
Number of Bonds	1700	740
Bond Yield	98.3 %	99.3%
Overall Yield	80.0%	99.3%

device has a probability of $Y_{1Bond} = 99.999\%$ to have no short and no open. The yield of the bond process ($Y_{Bonding}$) (table 4) is calculated with the following equation.

$$Y_{Bonding} = (Y_{1Bond})^{\#Bonds} \quad (4)$$

The SRAM on the Pentium MCM are not Known Good Dies ($Y_{Die} = 95\%$), therefore they influence the overall yield.

$$Y_{Overall} = Y_{dBonding} \cdot (Y_{Die})^{\#Dies} \quad (5)$$

On both types of substrate the bonding process was equally stable, that means the SMART-P5 module with less bonds will show a higher yield, which results in lower overall costs. Though process flow for the production of the SMART-P5 module is more complex, we expect it to be clearly the cheaper solution.

5 Status

Both modules have been successfully produced, and the prototypes have been tested in system. The function of the MCM-D module has been demonstrated in an industrial PC on an Euro Board. As the package is specially designed for this MCM by IMEC, the MCM goes through a detailed reliability analysis and qualification. The SMART-P5 runs in an industry PC by Digital-Logic AG on a PC/104 board. Digital-Logic AG is now doing the redesign for series production. This redesign will use the latest low power version of the Pentium Processor, which will further improve the thermal behavior of the module. First series are expected in first quarter 1998.

6 Outlook

A qualification of the production processes for the existing prototypes is planned in the near future. Also a reliability analysis will be done, which will show weak spots in the existing design and how to avoid these traps in future designs. These reliability analysis

will also give the opportunity to compare the reliability of these two build-up technologies. Furthermore, a realisation of the MCM-D module using Flip-Chip technology would allow to reduce the size and performance of the module even more and parallelly reduce production cost.

References

- [1] P. Eggenberger, M. Dietz, J.-P. Wyss, and E. Hirt. *SMART-P5 - Project Documentation*. 1997.
- [2] E. Hirt et al. *A Pentium based MCM for Embedded Computing*. 1997.

²without SMT process cost

³Known Good Dies