Early Footprint Estimation for Area I/O Packages

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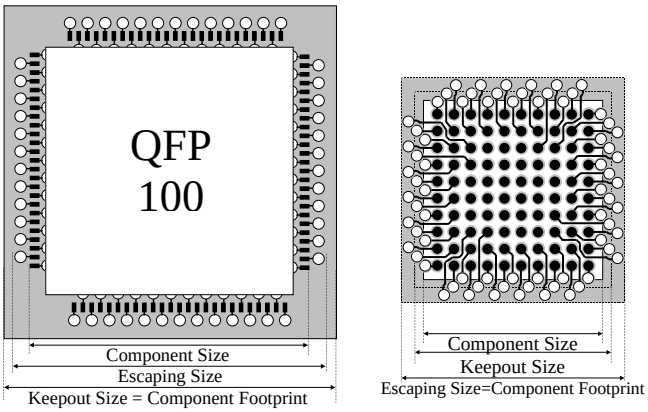
1 Introduction

Area array packages such as ball grid arrays (BGAs), fine-pitch BGAs (FP-BGAs) [1] and chip scale/size packages (CSPs)[2] become more and more popular because they allow smaller systems without using bare die attach. Thus, system designers are faced with more and more ICs that are only available in area array packages. Next to the difficulty of visual inspection, the requirements for the PCB are growing. So, a QFP is easy to escape with standard design rules. But a BGA with 1 mm pitch has a large escaping overhead, so that the package footprint is much larger than the package itself (figure 1) and the escaping can dominate the spacing between two components. Furthermore, a FP-BGA with 0.75 mm pitch is even unroutable on a standard PCB because the fanout can not be done on the top layer and the via lands are to large to escape the inner rows to an inner layer.



(a) QFP100 with 0.5 mm Pitch

(b) BGA100 1 mm Pitch

Figure 1: Escaping from pads (black) on a PCB with 125/125/650 for QFP 100, FPBGA 100. The vias are unfilled circles.

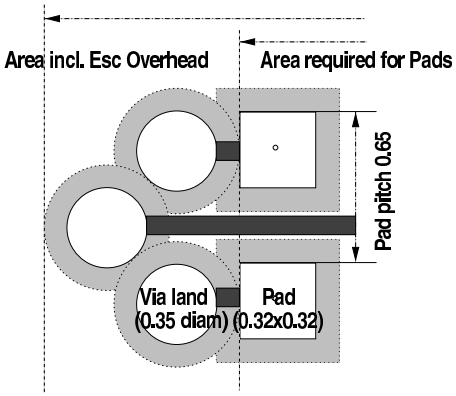


Figure 2: Overhead for single 100 μm wide line escaping (black) from area I/O with 0.65 mm pad pitch to vias (unfilled circles) with 350 μm diameter and 100 μm spacing (gray)

These problems can be solved by adding one or several built-up layers onto a PCB core[3]. They provide much smaller via lands using photo or laser drilling techniques.

Which packages to use and what type of substrate with how many layers is needed should be decided early in the design cycle before any layout is done. This top-down methodology leads directly to an optimal implementation. So, layout optimizations can be done, from the beginning, with the suitable PCB technology.

After the definition of the footprint of a component in section 2, models are presented in section 3 that enable this approach. The models can also be used for layout automation. Finally, illustrative examples are presented in section 4.

2 Footprint

We define the footprint of a package

1. as the pure component area, i.e. its size;
2. plus the maximum of
    - either assembly keepout overhead, e.g. for the SMT placer;
    - or I/O escape overhead, i.e. additional space for escaping all chip I/Os to another layer (see Fig.2).

Whereas the component size and the assembly keepout overhead are easy to determine, the I/O fanout overhead is not simple to calculate. Escaping from the pads to the vias can consume significant area. Thus, it can dominate the spacing needed between two adjacent components. Moreover, this escape area is highly dependent on substrate technology and design rules as shown in figure 3. A 100-pin BGA with 1 mm I/O pitch is much smaller than a QFP, but it consumes large escaping area, so the package footprint is much larger than the package itself. This is due to the fact that each trace has to leave the top layer with a via to an inner layer in order to place more of more components as dense as possible. The escape routing not only needs area but can also block a number of layers under and next to the component for escaping from inner pads. It can define the number of layers needed even if the global routing could be done on less layers.

The models presented in the next section allow an early estimation of the footprint with minimal input data. To estimate the impact of the package type on the system size, our models calculate the footprint from given package descriptions (size, pitch and number of I/Os). They use a library where the available substrate technologies are specified. Second, the number of signal layers needed to escape a component is calculated and escape layout can be done automatically.

3 Models

As defined in section 2, the footprint is the maximum of the assembly keepout area and the area including the escaping (A_{Esc}). Whereas the assembly keepout area is

easily calculated as the component size plus the minimum assembly spacing needed between adjacent ones, the escaping area is the pad size (A_{Pads}) plus the area needed by the escaping overhead (O_{Esc}) as shown in equation 1.

$$A_{Esc} = (\sqrt{A_{Pad}} + O_{Esc})^2 \tag{1}$$

The escaping overhead depends on the pad pitch, the design rules and the ball locations as detailed and modeled in the subsections. The models for the effective footprint are based on the following principles:

3.1 Number of Layers

To avoid local congestions, it is very important to know the minimum number of layers required for escaping. It defines the number of layers needed if global routing could be done on less layers. In addition to the inner layers, the top layer can also be used for escaping even when in reality the top layer is often left unrouted to allow for dense component placement.

3.2 Escaping

For area usage each trace is modeled to leave the top layer with a via to an inner layer. The fanout of as many rows as possible is done on each layer. This minimizes the number of layers needed. Best is, if the routing density is high enough to escape all rows between the pads of the outermost row. Otherwise inner rows of pads have to stagger down to additional layers.

When the minimum via pitch is larger than the pads pitch divided by the number of escaping traces on the top ($l_{top-eff}$), the vias can be arranged in rows as illustrated in figure 3. The area needed depends on the substrate design rules, the via type and if vias are allowed in pads. Whereas standard PCB often only provides mechanically drilled through hole vias, the build-up layers have microvias which stagger down one layer per via. For the calculation of the escape area the vias are modeled to escape on one side of a pad row with k being the number of vias in one row. Between two vias of adjacent via rows the following number of lines has to pass:

- Through hole vias: k
- Staggered vias: $k-1$ for the last via and $k-2$ between diagonal vias.

The distance between two vias in one row (d_{Via}) depends on the number of lines between the vias. For staggered vias or microvias, no lines are needed between. Thus, the minimum distance should be used (2):

$$d_{Via-stagger} \geq D_{ViaLand} + D_{Space} \tag{2}$$

Through hole vias on the other side would block the whole area underneath the escaping. So, $L_{EscVia} > 0$ lines should pass between the vias as illustrated in

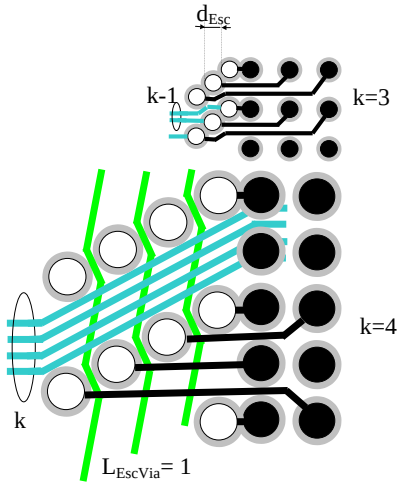


Figure 3: Escaping from BGA pads (black) with 0.7 and 1 mm pitch to vias (unfilled circles) with minimum spacing of 75/125 μm (grey) and to the outside on an inner layer (dark gray). The small vias are staggered microvias with a land diameter of 300 μm and the larger through hole vias have a land diameter of 650 μm

figure 3 and as calculated in formula 3:

$$d_{Via-through} = D_{ViaLand} + L_{Space} + L_{EscVia} * (L_{Space} + L_{Width}) \quad (3)$$

For both via types the number of escaping vias (k) has to be calculated first. Staggered vias can be put nearer together (4). Thus, k is lower than for through hole vias (5):

$$k_{stagger} \geq \frac{D_{ViaLand} - L_{Width}}{(P_{Ball}/l_{top-eff}) - L_{Space} - L_{Width}} \quad (4)$$

$$k_{through} \geq \frac{D_{ViaLand} + L_{Space}}{(P_{Ball}/l_{top-eff}) - L_{Space} - L_{Width}} \quad (5)$$

This escaping strategy is only possible if the escape pitches ($Pitch = P_{Ball}/l_{top-eff}$) are much larger than the line pitch. Otherwise, k would become very large. The escaping distance per additional via (d_{Esc}) is then calculated with (6) for through hole and (7) for staggered vias:

$$d_{Esc} = \sqrt{d_{Via}^2 - \left(\frac{d_{Via}^2 - [D_{ViaLand} + k * L_{Width} + (k+1) * L_{Space}]^2 + k^2 * Pitch^2}{2 * k * Pitch}\right)^2} \quad (6)$$

$$d_{Esc} = \sqrt{d_{Via}^2 - \left(\frac{d_{Via}^2 - [D_{ViaLand} + (k-2) * L_{Width} + (k-1) * L_{Space}]^2 + k^2 * Pitch^2}{2 * k * Pitch}\right)^2} \quad (7)$$

When the parameters k and d_{Esc} are calculated, the total escaping overhead is estimated using (8). In case vias are allowed in the substrate pads, the overhead is smaller, as shown in equation 9.

$$O_{Esc-NoVias} = 2 * [D_{ViaLand} + 2 * L_{Space} + (k-1) * d_{Esc}] \quad (8)$$

$$O_{Esc-ViasinPads} = 2 * ((k-1) * d_{Esc} + L_{Space}) \quad (9)$$

The number of rows that could be routed on the top layer (l_{top}) is the same as the number of lines between balls (l_{Pads}) plus one dependent on the pad diameter of the balls on the substrate (W_{Ball}) (10). The similar parameter for the inner layers (l_{in}) is calculated as the number of lines between two vias (l_{Vias}) placed in the same pitch as the ball pitch (P_{Ball}) plus one if inner rows can be escaped to another layer, otherwise it is 0 (11). Inner rows can be escaped when vias can be placed either into the pads or between them.

$$\begin{aligned} l_{Pads} &\leq \frac{P_{Ball} - W_{Ball} - L_{Space}}{L_{Width} + L_{Space}} \\ l_{top} &= l_{Pads} + 1 \end{aligned} \quad (10) \qquad \begin{aligned} l_{Vias} &\leq \frac{P_{Ball} - D_{ViaLand} - L_{Space}}{L_{Width} + L_{Space}} \; or \; 0 \\ l_{in} &= l_{Via} + 1 \; or \; 0 \end{aligned} \quad (11)$$

3.3 Full Area Array

To cover not only quadratic arrays, the two sides are distinguished. In the following equations N_l means the number of rows on the larger side, and N_s stands for the number of rows on the smaller side.On the top layer ($2 * l_{top}$) rows and $4 * (l_{top} - 1)^2$ pads can be escaped on the top layer. Additional 4 are escaped if lines can pass between the pads ($l_{top} > 1$). If inner balls can be escaped, the power balls (N_P) can be subtracted from the number of balls to escape. But N_P does not include the power balls in the outermost row as they are routed on the top layer anyhow. Thus, the number of remaining balls is given by:

$$N_{RemTop} = (N_l - 2l_{top})(N_s - 2l_{top}) - 4 * (l_{top} - 1)^2 - if(l_{top} > 1; 4; 0) - N_P \quad (12)$$

The component can be escaped if all balls are escaped on the top layer or if inner rows can be escaped by vias. Based on equation 13 the number of layers is calculated with (14).

$$\begin{aligned} e_{top} &= if(l_{top} > 1; 4; 0),\; e_{in} = if(l_{in} > 1; 4; 0) \\ N_{Rem} &= (N_l - 2l_{top} - 2nl_{in}) * (N_s - 2l_{top} - 2nl_{in}) - 4 * (l_{top} - 1)^2 \\ &\quad -4n(l_{in} - 1)^2 - e_{top} - n * e_{in} - N_P \\ a &= 4 * l_{in}^2 \\ b &= -2 * l_{in} * (N_l + N_s - 4l_{top} - 4 + 2l_{in}) - 4 - e_{in}) \\ c &= N_l * N_s - 2 * l_{top} * (N_l + N_s - 4) - 4 - e_{top} - N_P \\ n &\geq \frac{-b - \sqrt{b^2 - 4 * a * c}}{2 * a} \\ N_{Layer} &= n + 1 \end{aligned} \quad (13) \quad (14)$$

When inner layers are needed for escaping, less than the maximum possible number of rows (l_{top}) may be escaped on the top layer (15). Finally, the escaping size is given by (16).

$$l_{top-eff} \geq \frac{4n^2(l_{in})^2 - 2nl_{in} * (N_l + N_s - 4 + 2l_{in}) - 4n - 4 + N_l * N_s - N_P - ne_{in} - e_{top}}{2 * (N_l + N_s - 4 - 4nl_{in})} \quad (15)$$

$$A_{Esc} = ((N_l - 1) * P_{Ball} + W_{Ball} + O_{Esc}) * ((N_s - 1) * P_{Ball} + W_{Ball} + O_{Esc}) \quad (16)$$

3.4 Partial Array with Empty Center

Area Array with depopulated center are more common and can be divided into two types: with an empty center or having a small array of balls in the empty center. The center area is parameterized by the missing rows in the large (N_{lE}) and the small (N_{sE}) direction. Thus the number of missing balls including a possible center array is $N_{lE} * N_{sE}$. We first consider an empty center as shown in figure 4. To escape as many vias as possible into an empty center of area pads we do

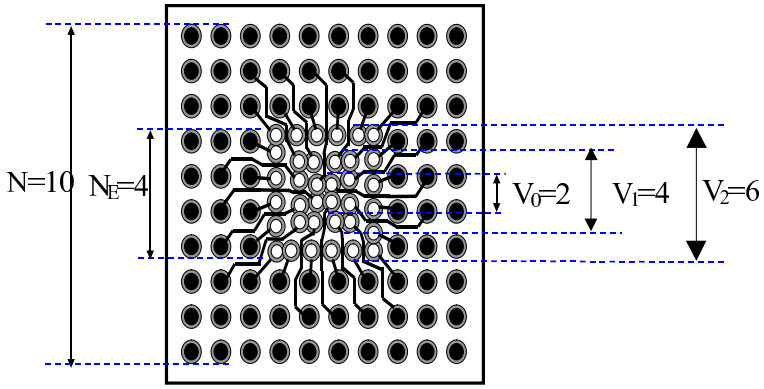


Figure 4: Arranging staggered vias in the empty area of a BGA

not use a fixed via grid but place them as densely as possible. First the model for a square empty center of N_E^2 missing balls is explained. Here four vias can be placed in the middle with minimal distances as shown in figure 4 as no line has to pass between. Thus, the number of vias in the first row (V_0) is two, the number of vias to escape from inside this first row (E_{-1}) is 0. For the rows, this number can be calculated with (17). Every row is at least two times the minimum via grid and two times the line pitch wider than the preceding one. The number of its vias depends on this width, the number of lines to escape (E_{n-1}) from the predecessors and the via pitch (18):

$$\begin{aligned} V_0 &= 2 \\ E_{-1} &= 0 \\ E_n &= E_{n-1} + N_n - 1 \qquad (17) \\ V_n &\geq \frac{(V_{n-1}+2)(D_{ViaLand}+L_{Space}) + L_{Space} + (E_{n-2}+2-E_{n-1})(L_{Width}+L_{Space})}{D_{ViaLand}+L_{Space}} \qquad (18) \end{aligned}$$

The width of the row (W_n) is then calculated with (19). This width has to be smaller than the center area minus two times the space for one line to pass between the balls and the vias (20). As the via rows are simultaneously added on all four sides the number of escaped balls (E_{tot}) is four times E_n (21):

$$W_n = V_n * (D_{ViaLand} + L_{Space}) + L_{Space} + E_{n-1} * (L_{Width} + L_{Space}) \qquad (19)$$

$$W_n \leq N_E * P_{Ball} - W_{Ball} - 2 * (L_{Width} + L_{Space}) \quad (20)$$

$$E_{tot} = 4 * E_n \quad (21)$$

For a rectangular empty center where the missing balls are $N_{lE} * N_{sE}$, the number of starting vias depends on the ratio of N_{lE} and N_{sE}. The minimum for V_{s0} is one and V_{l0} is calculated with (22) or both are two as in the quadratic version. Furthermore, if the center is filled in one direction, some space may be left for vias in the other. In this case, the number of vias is calculated in (23) as the maximum width is now defined from the empty area width (20):

$$V_{l0} \geq \frac{V_{s0} * N_{lE}}{N_{sE}} \quad (22)$$

$$V_n \geq \frac{N_E * P_{Ball} - W_{Ball} - (E_{n-1} + 2)(L_{Width} + L_{Space})}{D_{ViaLand} + L_{Space}} \quad (23)$$

When the number of balls that can be escaped in the center (E_{tot}) is calculated, it has to be checked if this number can be escaped from the rows to the center. Equation 24 shows that the maximum is given by the number of rows that can be escaped on the top (l_{top}) minus 4 times $l_{top}^2 - 1$ balls that can not escape because they are situated in the corners. The number of layers used for escaping is then calculated by using the full array equation 14. Here N_P is enlarged by E_{tot} and the number of depopulated balls $N_{lE} * N_{sE}$ (25):

$$E_{tot} = \min(E_{tot}; (N_{sE} + 2 * l_{top})(N_{lE} + 2 * l_{top}) - N_{lE}N_{sE} - 4 * (l_{top}^2 - l)) \quad (24)$$

$$N_{Layer} = n(N_P = N_P + E_{tot} + N_{lE} * N_{sE}) + 2 \quad (25)$$

3.5 Partial Array with Array in Empty Center

If the depopulated center is filled with an array of $N_{lI} * N_{sI}$ balls, the area for escaping is calculated using the equations for full array for the escaping overhead O_{Esc} calculation. Equation 26 then calculates the needed area (A_{center}). If it is larger than the total inner area including the center balls (A_{emtpy}), l_{top} has to be reduced for escaping calculation. This costs additional layers.

$$A_{center} = ((N_{lI} - 1) * P_{Ball} + O_{Esc}) * ((N_{sI} - 1) * P_{Ball} + O_{Esc}) \quad (26)$$

$$A_{empty} = N_{lE} * (P_{Ball})^2 * N_{sE} \quad (27)$$

If there is some space left after escaping the center array, vias can be placed similarly as in subsection 3.4. The number of vias to start with (V_{l0}, V_{s0}) is calculated from the width of the center area already used (28). The number of layers used is then calculated as equation 25 plus the number of layers used for the center array escaping ($n_{center} + 1$) as shown in equation 29.

$$V_0 = \frac{(N_I - 1) * P_{Ball} + W_{Ball} + O_{Esc} + 2 * (D_{ViaLand} + L_{Space})}{D_{ViaLand} + L_{Space}} \quad (28)$$

$$N_{Layer} = n(N_P = N_P + E_{tot} + N_{lE} * N_{sE}) + 2 + n_{center} + 1 \quad (29)$$

4 Examples

To demonstrate the model we consider an IC with 100 pins. This IC will be packaged into a QFP and BGAs with 1, 0.75 and 0.5 mm pad pitch. The packages are then mounted on a standard PCB as well as on sequential built-up layers (SBU). The substrate design rules are summarized in table 2. In these examples the minimum distance between adjacent components is 2 mm. The summary of the comparison is presented in table 1 and the results are discussed in the subsections below.

Table 1: Package footprint for different packages and substrates

	QFP	BGA A		BGA B	BGA B2	BGA C	BGA C2
Pitch [mm]	0.5	1		0.75	0.75	0.5	0.5
Pad Size [mm]	0.3	0.5		0.4	0.4	0.3	0.3
Array	n/a	10*10		10*10	14*15	10*10	14*15
Empty center	n/a	full		full	10*11	full	10*11
Substrate	PCB	PCB	SBU	SBU	PCB	SBU	SBU
Package Size [mm^2]	256	112		66	133	34	65
Fanout Overhead [mm]	1.6	5.9	1.2	0.9	3.1	0.9	0.9
Keepout Size [mm^2]	**324**	159	**159**	**102**	183	**61**	**101**
Fanout Size [cm^2]	310	**240**	116	66	**185**	34	65
Nr of Layers for Escaping	2	2	1	2	2	3	2

Table 2: Substrate parameters

Substrate Type	L_{Width} [μm]	L_{Space} [μm]	$D_{ViaLand}$ [μm]	Max Nr of Layers
PCB	125	125	650	30
SBU	75	75	300	3

4.1 QFP

The QFP is easy to mount as its footprint is dominated by component size and the keepout needed as shown in figure 1(a). The escaping can then be done on one or two layers. But it has by far the largest footprint of all examples.

4.2 BGA A (1 mm Pad Pitch)

A full array with 1 mm pad pitch is less than half the size of a QFP. And it can be routed on two layers on a standard PCB. However, due to the concentration of the I/Os on a small pitch and its large vias, a huge escaping overhead of about 6mm has to be paid. Thus, the footprint is nearly as large as the QFP package size. As

only one trace can pass between the vias, only two rows ($l_{top} = 2$) are escaped on the top layer. The rest can escape on a second layer which can be reached as the via lands fit between the balls. To reduce the footprint to the keepout size one build-up layer is sufficient.

4.3 BGA Bx (0.75 mm Pad Pitch)

By reducing the pad pitch the package can be made smaller (B). But a full array is not routable on a PCB because no vias can be placed between the pads. At the cost of two SBUs this package can be used with a footprint dominated by the keepout.

Another approach is to use a BGA with an empty center area. On a PCB no trace can pass between these balls. Therefore, we can only use a ring of two rows. The minimum size providing 100 balls is a BGA of 12*13 ($N_s * N_l$) balls with an empty center of 10*11 ($N_{sE} * N_{lE}$). Equation 21 shows that all inner balls can be escaped into the center. As shown in table 1 this package (B2) has about the same footprint as package A with one SBU. Thus, package B2 is preferred.

4.4 BGA Cx (0.5 mm Pad Pitch)

A full array with a 0.5 mm pad pitch (C) is still routable on SBU because vias can be put between the balls. It is even possible to put them into the pads. Its very small footprint is dominated by the keepout area. In fact it is only a fourth of the BGA A mounted on PCB. But it needs three SBU layers which rends the substrate expensive.

To reduce the area usage the center is depopulated in version C2. It needs the same depopulated center as B2 as no SBU trace can pass between the balls. This depopulation saves one SBU layer, but the package has about the same footprint as B mounted on SBU. Therefore, B is prefered as it provides much better assembly yield.

4.5 Intermediate Results

In table 3 the calculated intermediate results are summarized. It can be seen that k for the BGA A is quite high which is the reason for the large escaping overhead. For the BGAs with the depopulated center 46 vias have to be placed in the empty area. For the B2 three rows with 2,5,6 vias are used and on one side another 6 vias are added. Thus, the needed number just fits into the empty area. In the smaller empty center of C2 more vias could be placed due to the smaller via lands and line pitches. But as no line can pass between the pads, only the innermost row with its 46 pads can be reached.

Table 3: Intermediate Results for Package Comparison

Substrate	QFP PCB	BGA A PCB	BGA A SBU	BGA B SBU	BGA B2 PCB	BGA C SBU	BGA C2 SBU
E_{tot} (effectiv)	n/a	n/a	n/a	n/a	46(46)	n/a	64(46)
$l_{top-eff}$	1	2	3	1	2	1	1
l_{inner}	n/a	2	5	3	1	1	1
k	1	4	2	1	1	1	1
d_{Esc} [μm]	n/a	685	172	n/a	659	n/a	n/a

5 Summary and Outlook

Area I/O packages enable a size reduction if considered carefully. By performing the package and substrate selection early in the design cycle, a cost effective solution can be found. This early consideration represented up to now a lot of manual work. Thanks to the presented models it can be accomplished in much shorter time, considering more alternatives and exploring them in more detail. Thus, the number of needed build-up layers is known before layouting and may be avoided by an alternative package selection.

More models covering other package types and bare die attach can be found in [4]. These models also serve for layout automation and are the basis for the development of routing estimations suitable for high density packaging.

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