

# Early Footprint Comparison for Area I/O Packages and First Level Interconnect

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## Abstract

High density packaging (HDP) has a big potential for performance increase and size reduction as well as cost saving. To gain profit from this potential a careful package/first level interconnect and substrate selection is necessary. This selection defines the footprint of components and the number of layers needed to escape from them. The footprint not only includes the area needed for the pad placement but also the area used for each trace to leave the top layer with a via to an inner layer. Thus, it can dominate the spacing needed between two adjacent components. The number of layers for escaping defines the number of layers needed for the substrate if global routing could be done on less layers.

These two key figures allow to estimate the advantages and the cost of a solution. In this paper we present models to calculate them. Thus, these models can be used to determine the feasible implementations as well as its associated cost.

## 1 Introduction

The advantages of bare die attachment with regard to electrical performance and reduced mounting area are well known. For first-level interconnect - the electrical and mechanical connection from IC to any next level (substrate or package) - wire-bond, tape automated bonding (TAB) or Flip Chip (FC) can be used. These interconnects are well experienced and have low cost but the drawbacks of technologies are high manufacturing constraints for next interconnect layer (due to their fine I/O pitch) and the difficulty of testing the die before shipping[4].

A viable alternative are chip size/scale packages (CSP)[12] and fine pitch BGAs (FPBGA)[1] because these second level interconnect<sup>1</sup> match the fine on-chip pad pitch to an area arrangement with increased pitch. This increased pitch results in relieved substrate manufacturing constraints and eases die test as test sockets can be used.

On the other hand, these CSP/FPBGA packages require more area than bare die attach, and they are more expensive than standard QFP/BGA packages. This is especially true when an IC is not already available as CSP/FPBGA, so a custom package has to be designed which raises the issue of economical feasibility.

Whereas the electrical performance of CSP and FPBGA is

<sup>1</sup>The die is attached with a first level interconnect to a package (second level interconnect).

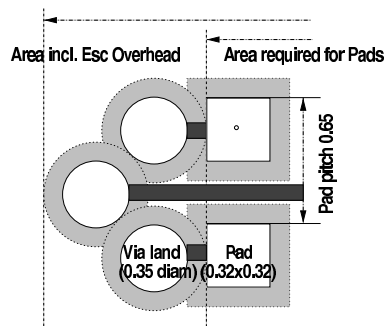


Figure 1: Overhead for single 100  $\mu\text{m}$  wide line escaping (black) from area I/O with 0.65 mm pad pitch to vias (unfilled circles) with 350  $\mu\text{m}$  diameter and 100  $\mu\text{m}$  spacing (grey)

similar to bare die attachment, cost savings depend on the availability of the package and its footprint because cost is a tradeoff between more layers and more area. This footprint is defined in section 2. And in section 3 we present models that allow an early estimation of the footprint as well as the number of signal layers needed for escaping a component. Finally, examples are presented in section 4. .

These models can be used to determine the feasible implementations in terms of package type or first level interconnect, substrate design rules, size and number of signal layers. With these data, a cost comparison can be performed using the MOE tool [10]. Furthermore, the calculated data and the models can also be used for layout automation.

## 2 Footprint

We define the footprint of a package or a first level interconnect

1. as the pure component area, that is its size;
2. plus the maximum of
  - either assembly keepout overhead, e.g. required for a wire-bonder, a flip-chip underfill tool, a placer;
  - or I/O escape overhead, i.e. additional space for escaping all chip I/Os to another layer (see Fig.1).

Whereas the component size and the assembly keepout overhead are easy to determine, the I/O fanout overhead is not simple to calculate. Escaping from the pads to the vias can consume significant area. Thus, it can dominate the spacing needed between two adjacent components. Moreover, this escape area is highly dependent on substrate technology and design rules as shown in figure 2.

An 100-pin QFP is easy to escape with standard design rules ( $125/125/650^2$ ) but consumes large footprint area. A 100-pin BGA with 1 mm I/O pitch has a much smaller size, but it consumes large escaping area, so the package footprint is much larger than the package itself. This is due to the fact that each trace has to leave the top layer with a via to an inner layer. The

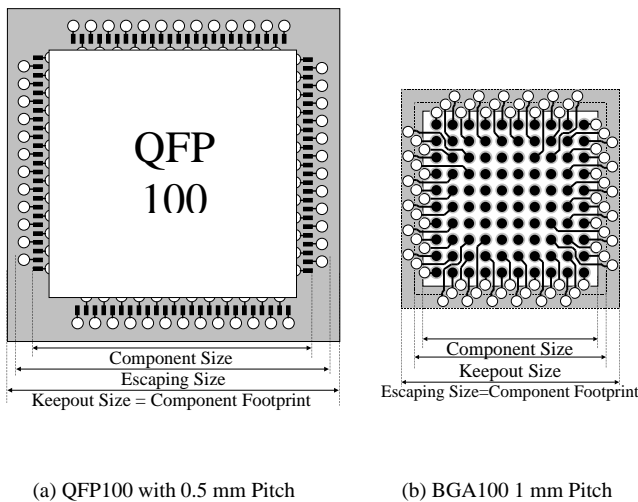


Figure 2: Escaping from pads (black) on a PCB with 125/125/650 for QFP 100, FPBGA 100. The vias are unfilled circles.

escape routing not only needs area but it can also block a number of layers under and next to the component for escaping from inner pads. It can define the number of layers needed even if the global routing could be done on less layers.

Existing footprint estimation tools such as Audit[2], Impact[5] and Savansys[9] and their routing estimations do not consider local layer congestions and local layer usage. Furthermore, these tools need a huge amount of data to be specified, and the build-up (first and second level interconnect, substrate, etc.) has to be defined by the user before any calculation can be done. It is very toilsome to assess two or more different implementations against each other because optimizations mainly rely on user corrections. Thus, they lack a robust routing optimization. Therefore, these software tools are not well suited for a tradeoff analysis considering all types of physical build-ups.

Our models allow an early estimation of the footprint with minimal input data. To estimate the impact of the first-level interconnect on the system size, our models calculate the footprint from given die or package descriptions (size, pitch and number of I/Os). They use a library where the available package and

substrate technologies are specified. Second, the number of signal layers needed to escape a component is calculated and escape layout can be done automatically.

### 3 Models

As defined in section 2, the footprint is the maximum of the assembly keepout area and the area including the escaping ( $A_{Esc}$ ). Whereas the assembly keepout area is easily calculated as the component size plus the minimum assembly spacing needed between adjacent ones, the escaping area is the pad size ( $A_{Pads}$ ) plus the area needed by the escaping overhead ( $O_{Esc}$ ) as shown in equation 1.

$$A_{Esc} = (\sqrt{A_{Pad}} + O_{Esc})^2 \quad (1)$$

The escaping overhead depends on the bonding method used as detailed and modeled in the subsections. These models for the effective footprint are based on the following principles:

#### Number of Layers

To avoid local congestions, it is very important to know the minimum number of layers required for escaping. It defines the number of layers needed if global routing could be done on less layers. Beside the inner layers, the top layer is also allowed for escaping even when in reality the top layer is often left unrouted to allow a dense component placement.

#### Escaping

For the area usage each trace is modeled to leave the top layer with a via to an inner layer. For components or interconnects that need several pad rows, such as wire bond, area flip chip and BGA, the fanout of as many rows as possible is done on each layer to minimize the number of layers needed. Best is when the routing density is high enough that all rows can escape between the pads of the outermost row. Otherwise inner rows have to stagger down to additional layers.

The escaping of the outermost row is always routed to the outside of a component. Inner wire bond rows or single pad rows can be escaped to both sides. Area pads are routed to the outside on a minimum number of layers. If the array center is depopulated, the innermost rows can be escaped to this free space. This is important when the pad pitch is too small to place vias between the pads.

When the via lands are larger than the pads and escaping alternating to both sides is not possible or not sufficient, vias can be arranged in rows as illustrated in figure 3. The effective area needed depends on the via type (through hole or staggered) and if vias are allowed in pads. For the calculation of the escape area the vias are modeled to escape on one side of a pad row with  $k$  being the number of vias in one row. Between two vias of adjacent via rows the following number of lines has to pass:

- Through hole vias:  $k$
- Staggered vias:  $k - 1$  for the last via and  $k - 2$  between diagonal vias.

The distance between two vias in one row ( $d_{Via}$ ) depends on the number of lines between the vias. For staggered vias or microvias there is no need for lines between. Thus, the minimum

<sup>2</sup>line/space/via land, all measures in micron

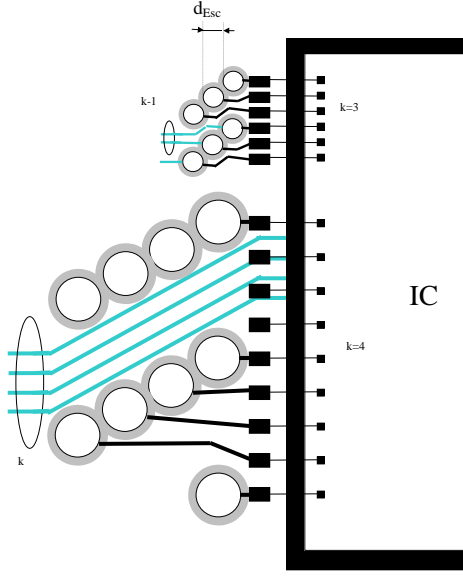


Figure 3: Escaping from wire bond pads (black) with 225 and 500  $\mu\text{m}$  pitch to vias (unfilled circles) with minimum spacing of 75/125  $\mu\text{m}$  (grey) and to the outside on an inner layer (dark gray). The small vias are staggered microvias with a land diameter of 300  $\mu\text{m}$  and the larger through hole vias have a land diameter of 650  $\mu\text{m}$

distance should be used (2):

$$d_{Via-stagger} \geq D_{ViaLand} + D_{Space} \quad (2)$$

Through hole vias on the other side would block the whole area underneath the escaping. So,  $L_{EscVia} > 0$  lines should pass between the vias as illustrated in figure 3 and as calculated in formula 3:

$$d_{Via-through} = D_{ViaLand} + L_{space} + L_{EscVia} * (L_{Space} + L_{Width}) \quad (3)$$

For both via types the number of escaping vias ( $k$ ) has to be calculated first. Staggered vias can be put nearer together (4). Thus  $k$  is lower than for through hole vias (5). Here the *Pitch* is the bondpad pitch or the ball/bump pitch divided by the number of lines passing between the ball/bumps:

$$k(Pitch) \geq \frac{D_{ViaLand} - L_{Width}}{Pitch - L_{Space} - L_{Width}} \quad (4)$$

$$k(Pitch) \geq \frac{D_{ViaLand} + L_{Space}}{Pitch - L_{Space} - L_{Width}} \quad (5)$$

This escaping strategy is only possible if the escape pitches are much larger than the line pitch. Otherwise,  $k$  would become very large. The escaping distance per additional via ( $d_{Esc}$ ) is then calculated with (6) for through hole and (7) for staggered vias.

When the parameters  $k$  and  $d_{Esc}$  are calculated, the total escaping overhead is estimated using (8). Or if vias are allowed in the substrate pads the overhead is smaller, as shown in formula 9:

$$O_{Esc-NoVias} = 2 * [D_{ViaLand} + 2 * L_{Space} + (k - 1) * d_{Esc}] \quad (8)$$

$$O_{Esc-ViasinPads} = 2 * ((k - 1) * d_{Esc} + L_{Space}) \quad (9)$$

### Area Flip Chip and BGA

Flip Chip as well as BGA concentrate the I/Os on a small area. This concentration of many I/Os needs area for escaping, thus enlarging the footprint significantly. Additionally, the bump/ball pitch ( $P_{Bump}$ ) has to be larger than the wiring pitch to allow escaping from inner rows for full area connection. All rows are escaped on the top layer if possible. Thus, as few layers as possible are used. This strategy enlarges the footprint because these I/Os have to be routed from the top to an inner layer as illustrated in figure 4.

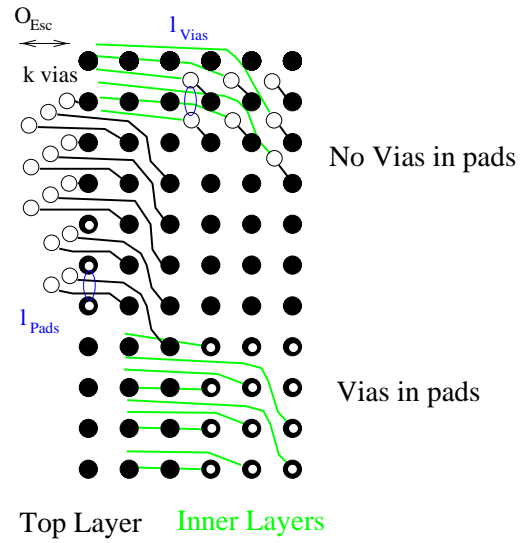


Figure 4: Escaping from Area Pads (black) to vias (unfilled circles)

The number of rows to be routed on the top layer ( $l_{top}$ ) is the same as the number of lines between bumps ( $l_{Pads}$ ) plus one dependent on the pad diameter of the bumps on the substrate ( $W_{Bump}$ ) (10).

$$l_{Pads} \leq \frac{P_{Bump} - W_{Bump} - L_{space}}{L_{width} + L_{space}} \quad (10)$$

$$l_{top} = l_{Pads} + 1$$

The similar parameter for the inner layers ( $l_{in}$ ) is calculated as the number of lines between two vias ( $l_{Vias}$ ) placed in the same pitch as the bump pitch ( $P_{Bump}$ ) plus one if inner rows can be escaped to another layer, otherwise it is 0 (11). Inner rows can be escaped when either vias can be placed into the pads or between them.

$$l_{Vias} \leq \frac{P_{Bump} - D_{ViaLand} - L_{space}}{L_{width} + L_{space}} \text{ or } 0 \quad (11)$$

$$l_{in} = l_{Vias} + 1 \text{ or } 0$$

$$d_{Esc-through} = \sqrt{d_{Via}^2 - \left( \frac{d_{Via}^2 - [d_{ViaLand} + k * l_{width} + (k+1) * l_{space}]^2 + k^2 * Pitch^2}{2 * k * Pitch} \right)^2} \quad (6)$$

$$d_{Esc-stagger} = \sqrt{d_{Via}^2 - \left( \frac{d_{Via}^2 - [d_{ViaLand} + (k-2) * l_{width} + (k-1) * l_{space}]^2 + k^2 * Pitch^2}{2 * k * Pitch} \right)^2} \quad (7)$$

To cover not only rectangular arrays, two numbers of rows are distinguished. In the following equations  $N_l$  means the larger number of rows and  $N_s$  stands for the smaller side.

On the top layer ( $2 * l_{top}$ ) rows and  $4 * (l_{top} - 1)^2$  pads can be escaped on the top layer. Additional 4 are escaped if lines can pass between the pads ( $l_{top} > 1$ ). And if inner bumps can be escaped, the power bumps  $N_P$  can be subtracted from the number of bumps to escape. But,  $N_P$  does not include the power bumps in the outermost row as they are routed on the top layer anyhow. Thus the number of remaining bumps is given by:

$$N_{RemTop} = (N_l - 2l_{top})(N_s - 2l_{top}) - 4 * (l_{top} - 1)^2 - if(l_{top} > 1; 4; 0) - N_P \quad (12)$$

The component can be escaped if all bumps are escaped on the top layer or if inner rows can be escaped by vias. Based on formula 13 the number of layers is calculated with (14).

$$\begin{aligned} e_{top} &= if(l_{top} > 1; 4; 0), e_{in} = if(l_{in} > 1; 4; 0) \\ N_{Rem} &= (N_l - 2l_{top} - 2nl_{in}) * (N_s - 2l_{top} - 2nl_{in}) - 4 * (l_{top} - 1)^2 - 4n(l_{in} - 1)^2 - e_{top} - n * e_{in} - N_P \\ a &= 4 * l_{in}^2 \\ b &= -2 * l_{in} * (N_l + N_s - 4l_{top} - 4 + 2l_{in}) - 4 - e_{in} \\ c &= N_l * N_s - 2 * l_{top} * (N_l + N_s - 4) - 4 - e_{top} - N_P \\ n &\geq \frac{-b - \sqrt{b^2 - 4 * a * c}}{2 * a} \\ N_{Layer} &= n + 1 \end{aligned} \quad (14)$$

When inner layers are needed for escaping may less than the maximum possible number of rows ( $l_{top}$ ) be escaped on the top layer. The effective number of rows ( $l_{top-eff}$ ) is calculated with (16). Thus the pitch of lines escaping from the pads ( $Pitch$ ) is  $P_{Bump}/l_{top-eff}$ . Putting it into (4) or (5)  $k$  is calculated as (16). With the same pitch the escaping overhead ( $O_{Esc}$ ) is obtained with (17). And finally the escaping size is given by (18).

$$k \geq \frac{D_{ViaLand} + L_{Space}}{P_{Bump}/l_{top-eff} - L_{Space} - L_{Width}} \quad (16)$$

$$O_{Esc} = Overhead(Pitch = P_{Bump}/l_{top-eff}) \quad (17)$$

$$A_{Esc} = ((N_l - 1) * P_{Bump} + W_{Bump} + O_{Esc}) * ((N_s - 1) * P_{Bump} + W_{Bump} + O_{Esc}) \quad (18)$$

### TAB and Peripheral Flip Chip

TAB as well as FC mounted dies with peripheral pads have their pads arranged in one row. This makes it possible to fanout

the row to both the in- and the outside of the component. Thus, the escaping area is smaller as  $k$  is reduced by the number of via rows that fanout to the inside  $k_1$ . This changes (8) to (19).

$$O_{Esc} = 2 * (D_{ViaLand} + 2 * L_{Space} + (k - 1 - k_1) * d_{Esc}) \quad (19)$$

### Wire Bonding

Wire bonding adds some overhead as substrate bond pads especially on laminates have to be larger than on the ICs. The pad size is adapted to allow for misalignment, the softer substrate and the larger footprint for the second bond for ball-wedge bonding. In this paper we only describe the model for orthogonal wire bonding because it is much simpler. The spreading model will be presented in a later paper.

For wedge-wedge bonding orthogonal wire-bonding is preferred, as turning the bond head costs time. Therefore, the minimum number of rows depends on the minimum on-chip pad pitch ( $C_{pp}$ ) versus the minimum feasible bondpad pitch on the substrate ( $BP_{width} + L_{space}$ ) as shown in formula 20. This is the worst case as the mean on-chip pitch is larger and slight spreading can be used. But, often there are depopulated areas, so a mean pitch calculation fails.

$$N_{Row} \geq (BP_{width} + L_{space})/C_{pp} \quad (20)$$

The spacing between two wire bond rows is calculated from the via land ( $D_{ViaLand}$ ), the line width and spacing ( $L_{Width}, L_{space}$ ) and the bondpad pitch. It mainly depends on the number of vias needed to reach the next layer without blocking it completely. The number of vias in one line to escape from one wire bond ( $k$ ) row can be estimated with formula 4 or 5 as illustrated in figure 3 using:

$$Pitch = \max(C_{pp}; BP_{width} + L_{space}) \quad (21)$$

The overhead is then calculated with equation 22 including the minimum bondpad to bondpad spacing ( $B_{space}$ ) of adjacent ICs.  $D_{Esc}$  is calculated from (6) or (7). The number of layers blocked for escaping is the same as the number of bondpad rows.

### 4 Footprint Examples

For the examples we consider a pentium processor with voltage reduction technology from Intel [8]. This component is available in an ceramic pin grid array (PGA), in a TAB package and as fully tested bare die (smart die). The die measures 9.1 mm by 9.9 mm and has 358 peripheral pads on a 75  $\mu$ m pitch. This IC is packaged virtually into standard package PGA, in a chip size package (CSP) and mounted using TAB, wire bond and flip chip (FC) as first level interconnect.

$$l_{top-eff} \geq \frac{4n^2(l_{in})^2 - 2nl_{in} * (N_l + N_s - 4 + 2l_{in}) - 4n - 4 + N_l * N_s - N_P - ne_{in} - e_{top}}{2 * (N_l + N_s - 4 - 4nL_{in})} \quad (15)$$

$$\frac{O_{Esc}}{2} = C_{height} + BP_{length} + \max\left(\frac{B_{space}}{2}; D_{ViaLand} + 2 * L_{Space} + k * d_{Esc}\right) \quad (22)$$

$$+ (N_{Row} - 1) * (BP_{length} + L_{space} + if(k > 0; D_{ViaLand} + L_{space}) + (k - 1) * d_{Esc})$$

These packages are placed on all generic types of substrate such as PCB, advanced PCB (MCM-L), conventional thick film (MCM-C) and thin film (MCM-D). Their wiring pitch ( $P_{w\text{eff}}$ ) range from 65  $\mu\text{m}$  to 510  $\mu\text{m}$ . It is calculated as the mean between the line and the via pitch as shown in formula (23) [7]. Their line width ( $L_{width}$ ), line space ( $L_{space}$ ), via land diameter ( $D_{ViaLand}$ ) and their minimum bond pad width ( $BP_{width}$ ) are summarized in table 2.

$$P_{w\text{eff}} = \frac{(L_{width} + L_{space}) + (D_{ViaLand} + L_{space})}{2} \quad (23)$$

### PGA

The processor is available in a 296 pin ceramic pin grid array measuring 50 by 50 mm. This package is easy to fanout even on a standard PCB. But its package size as well as the package parasitics are major drawbacks. In fact it consumes more than double the area as the next smaller first level interconnect TAB shown in table 1 and figure 5.

### TAB

Besides its large size due to the high number of pins the TAB mounting, figure 5(a), suffers from the large escaping overhead needed on substrates with lower interconnect density. Even when some pins escape under the body, the escaping overhead to be added to the package size is more than 8 mm per side. The assembly of TAB is not standard as special equipment has to be used.

### BGA

BGA packages are much smaller. When packaging the processor virtually in a BGA, we found that the package size would be 420 mm<sup>2</sup> at 1 mm ball pitch. This I/O defined size is only slightly larger than the size needed to wire bond the die onto the BGA interposer. When placing this package onto a PCB, the footprint is the size of the pads enlarged by the fanout overhead 543 mm<sup>2</sup> caused by the three via rows needed. Placed on an MCM-L the escaping size is smaller than the footprint because the space needed between adjacent components of 2 mm needs more area than escaping.

### Wire Bond

Wire bonding is the most mature and most widely used first level interconnect. It allows to match the die bond pad pitch to the much larger substrate bondpad pitch as long as the bond wires do not become too long. This substrate pitch is highly dependent on the technology as shown in table 2. Whereas the pad pitch ratio (on-chip vs. substrate) defines the number of wire bond rows, the design rules dominate the space needed between two rows to allow escaping to an inner layer. Thus, the fanout

overhead on an MCM-L is four times larger than on an MCM-D. As shown in table 3 this 8.7 mm overhead is due to three bond rows needed instead of two for thin film and the much larger spacings between caused by the vias. So, the footprint on an MCM-L is much larger than the die size (three times) whereas for an MCM-D it is only 50 % overhead as shown in figure 5(e) and 5(d). These figures are pictures of existing modules [7], [3].

### CSP and FC

The smallest possible footprint can be obtained with flip chip (FC) mounting. Our example is difficult to bond directly as the the bond pad pitch is too small. This can be overcome by adding a thin film layer onto the IC to re-route the peripheral pads to area interconnections, thus making a chip size package (CSP). This CSP has a much larger pitch of 430  $\mu\text{m}$ . It is not possible to escape this CSP on a PCB but the footprint is the same on an MCM-L and D as it is dominated by the minimum spacing between the chips (1mm). Obviously more layers are needed on an MCM-L.

The same footprint results for FC without re-routing. But it can only be bonded onto an MCM-D because of the very tight line pitch needed.

### Calculation Results

Table 3 specifies some more input data and shows the intermediate data for the calculation of the sizes in table 1. This data as well as the resulting sizes were calculated using the models presented in the previous section. It should be noted that for the TAB calculation  $k$  would be 11 if not  $k_1 = 5$  out of them were routed to the inside.

## 5 Summary and Outlook

In this paper we presented methods and models for virtually packaging and mounting components. This allows partitioning, substrate and bonding selection and cost modeling in an early stage of design [11]. Besides the model presented, a non orthogonal wire bonding model with bond pad alignment exists. Further details for BGA modeling can be found in [6]. These models also serve for layout automation and they are the basis for the development of routing estimations suitable for high density packaging.

### References

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Table 1: Processor footprint for different packages/first level interconnect and substrates

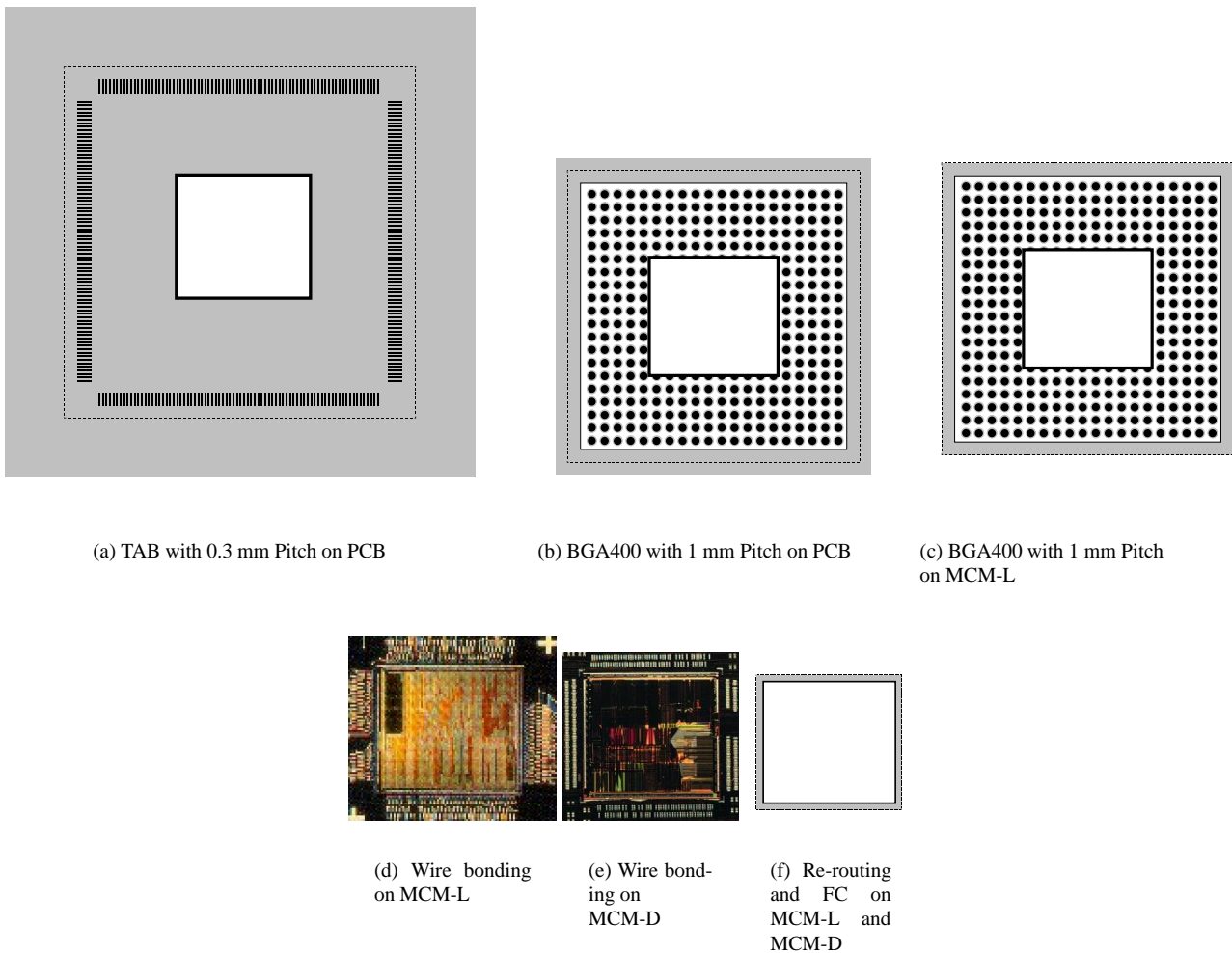
Substrate	PGA any	TAB PCB	BGA PCB	1 mm MCM-L	Wire MCM-L	bonding MCM-D	CSP MCM-L	0.43 mm MCM-D	FC MCM-D
Package Size [mm <sup>2</sup> ]	2500	676	420		90		90		90
Fanout Overhead [mm]	0	8.8	3.8	1.3	8.7	2.2	0.2	0	0.3
Keepout Size [mm <sup>2</sup> ]	<b>2704</b>	784	506	<b>506</b>	n/a	n/a	<b>110</b>	<b>110</b>	<b>110</b>
Fanout Size [mm <sup>2</sup> ]	2500	<b>1211</b>	<b>543</b>	433	<b>331</b>	<b>145</b>	94	90	97
Nr of layers for Escaping	1	2	2	1	3	2	3	1	1

Table 2: Generic substrate parameters

Substrate Type	$L_{width}$ [ $\mu\text{m}$ ]	$L_{space}$ [ $\mu\text{m}$ ]	$D_{ViaLand}$ [ $\mu\text{m}$ ]	$P_{w\text{eff}}$ [ $\mu\text{m}$ ]	$BP_{width}$ [ $\mu\text{m}$ ]
PCB	125	125	650	510	125
MCM-L	75	75	300	260	125
MCM-C	125	125	200	290	125
MCM-D	20	30	50	65	100

Table 3: Footprint calculations

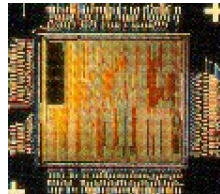
Substrate	PGA any	TAB PCB	BGA PCB	1 mm MCM-L	Wire MCM-L	bonding MCM-D	CSP MCM-L	0.43 mm MCM-D	FC MCM-D
Pad Pitch [ $\mu\text{m}$ ]	2540	300	1000		225	150	430		75
Pad width [ $\mu\text{m}$ ]	1000	100	620		150	100	250		60
Keepout [mm]	1	1	1	1	0.2		0.5		0.5
$l_{top\text{-}eff}$	3	n/a	2	3	n/a	n/a	1	3	n/a
$l_{inner}$	n/a	n/a	1	5	n/a	n/a	1	7	n/a
$k$	1	6	3	2	3	1	1	1	2
$d_{Esc}$ [ $\mu\text{m}$ ]	n/a	690	490	170	290	n/a	n/a	n/a	28



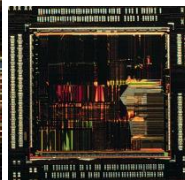
(a) TAB with 0.3 mm Pitch on PCB

(b) BGA400 with 1 mm Pitch on PCB

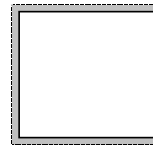
(c) BGA400 with 1 mm Pitch on MCM-L



(d) Wire bonding on MCM-L



(e) Wire bonding on MCM-D



(f) Re-routing and FC on MCM-L and MCM-D

Figure 5: Footprint comparison for mobile pentium processor die (white). The escaping size is the dashed box and the footprint size the grey box.

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