Assessing the Cost Effectiveness of Integrated Passives

Michael Scheffler, Gerhard Tröster
Electronics Lab, ETH Zurich, Gloriastr. 35, 8092 Zurich
Ph: +41 1 63 25829, Fx: 21210, eMail: scheffler@ife.ee.ethz.ch
http://www.ife.ee.ethz.ch/mcm/

Abstract

Passive components integrated into a high-density substrate can be a tolerable way to overcome the size and manufacturing limits of SMD passives mounted onto the system board. Still, this technology is perceived as being "too risky" and not cost effective. In this paper we propose a "passives optimized" solution combining the advantages from both SMD and integrated technology and avoiding the respective drawbacks. Exemplified by a GPS receiver front end, we present a methodology to assess the possible benefits when using the mixed technology.

1 Introduction

Passive components such as resistors, capacitances or inductors, are an integral part of every electronic subsystem present on today's market. They are not only inevitable for filters in RF systems, but they can also contribute up to 80% of the component count in purely digital systems as pull-ups or decoupling capacitors. As surface mount devices (SMDs), these components continue to shrink, but the surrounding space for mounting/soldering purposes ("footprint") can barely be further reduced (see Fig. 1 [6]).

Thus, during the last several years research activities have been underway to develop integrated passives (IPs), components which are part of the substrate/PCB and are fabricated with the same process as the substrate. The advantages of IPs are numerous. System manufacturers can achieve a reduction of process steps and assembly time. Moreover, IPs can lead to a significant size reduction of the overall system. Still, integrated passives have not made their way to the market, as some "show killers" remain attributed to them:

- In certain cases, the tolerances of integrated passives do not suffice for the target application.
- For decoupling capacitors, the dielectric materials used result in areas consumed several times as large as the area for the respective SMD component.
- The cost effectiveness of the IP technology is yet to be proven, as the cost for such a "smart substrate" is significantly higher than for a standard one.

Some rules of thumb do exist stating that for an arbitrary board size for more than 10 resistors the IP solution is more cost effective [2]. Even semi-automated approaches have been published recently coping with a trade-off between cost, size and resistor paste optimization [7]. But with these approaches the potential of the Integrated Passives technology cannot be fully assessed, as they do not take high performance passives as inductors and filters into account.

In this paper, we compare several possible implementations for a GPS receiver front end. This receiver has been a demonstrator application of the EU research project SUMMIT (Silicon Substrates Multichip Modules for Innovative Products) [1]. With our methodology, the optimum physical build-up for a given set of components can be determined in an easy and straightforward manner.

The remainder of this paper is organized as follows: in the next chapter, we briefly review the Integrated Passives technology for thin-film technology. Then, we describe the architecture of the case study, the GPS receiver, and the possible build-ups we deduced. Next, a performance/size/cost analysis for the implementations is performed using our methodology. Finally, the results are discussed.

2 The Integrated Passives technology

In principle, thin-film integrated passives use the same process steps as the metal interconnections.

Integrated resistor layers are sputtered, up to some 10nm thickness using typically CrSi or NiCr [4]. Resistors are realized as "normal" interconnection lines, for larger values a meander structure is used. Tolerances are about $\pm 15\%$, with laser tuning values below $\pm 1\%$ have been achieved [5]. For example, with a specific resistance of

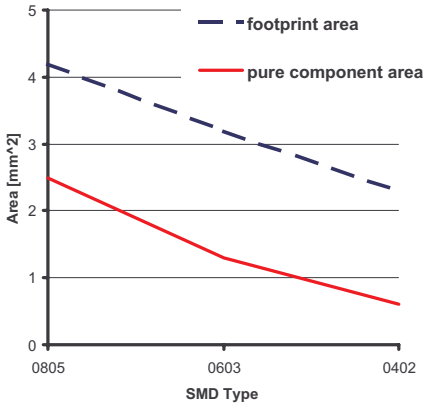

Figure 1. Area vs. SMD Type [6]

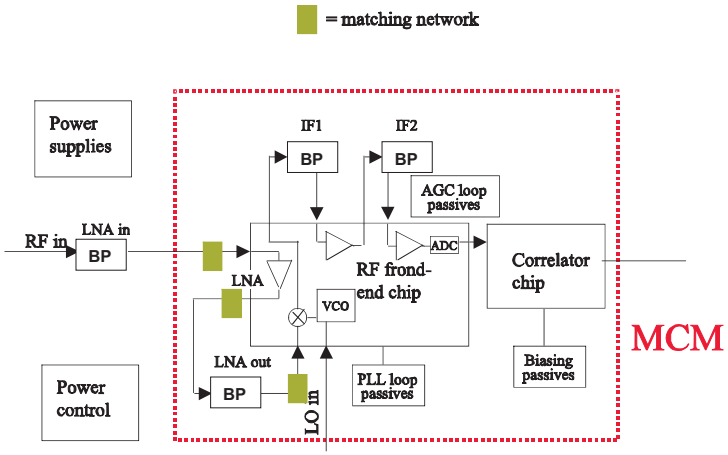

Figure 2. Schematic RF part of the GPS front end

360Ω/sq (CrSi) a 200Ω resistor would require an area of 0.01mm^2.

Integrated capacitors are fabricated by depositing a sandwich structure or interdigitated combs with a high κ material in the middle, e.g., Si_3Ni_4 or Ba_XTiO_Y. Thus, capacitors up to 100pF/mm^2 (10nF/cm^2) have been realized.

The development of **integrated inductors and filters** has been one of the main goals of the EU research project SUMMIT [3]. Inductors are realized as spiral-shaped interconnection lines, and the value is determined by the number of turns and the line width and line spacing. Next to high-Q inductors also bandpass filters in the Gigahertz-range have been implemented. They were realized as lumped elements consisting of single Rs, Ls, Cs.

3 A typical RF application: a GPS front end

One of the SUMMIT project demonstrators covered a global positioning system (GPS) receiver, an RF application requiring a large amount of precision filtering and matching networks. The chip set has been a new development from the project partner THOMSON-CSF DETEXIS.

For small, hand-held, low-power GPS systems, a reduction of size, cost, and power consumption is mandatory. Multichip-module (MCM) technology can be used to achieve these sophisticated constraints by offering a higher packaging density and better interconnect solutions.

A functional schematic of the GPS front end is shown in Fig. 2. The operation is roughly as follows: After external filtering, the GPS signal passes via a matched impedance line to a low-noise amplifier (LNA), and is filtered at 1.575GHz to reject the image frequency. Using a voltage controlled oscillator (VCO) to feed the internal reference, the signal is downconverted via intermediate frequencies (IF) to the base band. After A/D conversion, the signal undergoes the selection in the correlator and the subsequent stages.

Thus, in addition to the RF chip and DSP correlator, the following components are required:

- a band pass filter for 1.575GHz,
- 50Ω matching networks for the LNA and the mixer on the RF chip,
- IF band pass filters at 175MHz plus a PLL filter.

4 The trade-off problem

For this demonstrator, the challenge was to find the optimal implementation to realize the large amount of passives required for the GPS front end. As the filtering networks including decoupling and pull-up resistors require about 60 passive components, the use of integrated passives had to be evaluated. But the performance of the integrated filters was unclear, as shown in the last section, and integrated decoupling capacitors consume large substrate area. So, for these components a trade-off analysis between integrated and SMT passives was necessary.

Our methodology covers the following steps:

1) generate viable build-up implementations

2) assess performance with regard to the specifications

3) calculate the substrate area required

4) calculate the cost including test and yield aspects

5) make a decision

Table 1. Area-relevant data

Component	packaged		integrated passives(IP) /bare die			
RF Chip	TQFP:	225mm^2	wire bonded:	28mm^2	flip chip:	13mm^2
DSP Correlator	PQFP:	1165mm^2	wire bond:	88mm^2	flip chip:	59mm^2
Passives	0603:	3.75mm^2	IP-R (100kΩ)	0.25mm^2	IP-L (40nH)	1mm^2
	0805:	4.5mm^2	IP-C (50pF)	0.3mm^2		
Filter	SMD:	27.5mm^2	Integrated:	12mm^2	(3stage)	

$\Rightarrow$ Area MCM-Substrate: 1.1 * Total Area Components + 1mm edge clearance on either side
$\Rightarrow$ Laminate: Total Area Silicon Substrate + 5mm edge clearance on either side

Table 2. Cost and Yield data for Implementations 1 - 4 (chip cost is confidential)

		1	2	3	4
RF Chip	Cost/Yield	XX/99.9%	YY / 95% (Bare Die)		
DSP Correlator	Cost/Yield	ZZ/99.99%	AA / 99% (Bare Die)		
Substrate	Yield/cost per cm^2	99.99%/0.1	99%/1.75	90%/2.25	90%/2.25
Chip Assembly	Cost/Yield	0.15/93.3%	0.10/99%	0.10/99%	0.10/99%
Wire Bond	Cost/Yield	n/a	0.01/99.99%	n/a	n/a
	# Bonds		212		
SMD Assembly	Cost/Yield	0.01/99.99%	0.01/99.99%	n/a	0.01/99.99%
	# SMD's/Cost SMD's	112/11.0	112/8.6		12/2.6
Packaging	Cost/Yield	n/a	7.30/96.8%	4.70/96.8%	3.50/96.8%
Final test	Cost/Fault Coverage	10/99%	10/99%	10/99%	10/99%

4.1 Possible build-ups and their performance

Next to standard wire bond and the integrated passive technologies, we also benchmarked flip chip as the first level interconnect, to reduce the area needed for interconnection and to improve signal integrity.

This leads to three MCM implementations plus a PCB reference to be evaluated:

1: reference full PCB solution (PCB/SMD)

2: standard solution featuring wire bond as die-to-substrate interconnect and mounting SMD components as passives (MCM-D(Si)/WB/SMD),

3: flip chip and integrated passives leading to less footprint area consumed by the dies, higher costs and lower yield for the substrate (MCM-D(Si)/FC/IP),

4: flip chip and passives optimized taking into account that in case SMD components consume less area than integrated passives, the SMD component is preferred (MCM-D(Si)/FC/IP&SMD).

The entire analog processing chain from RF input to correlator input had to be implemented. The LNA output filter can use integrated passives only. Its main function is to reject the image frequency at 1.225GHz. Being of Cauer type it achieves a good rejection at the image frequency and has losses of 3 dB at the GPS signal frequency (1.575GHz), meeting the performance specifications. Matching networks of the LNA output and of the mixer input could also be integrated into the substrate leading to a direct connection from the LNA to the mixer.

The original specifications for the IF filters cannot be met with the integrated passives only. The quality factor of SUMMIT passives is quite good in the 1-2GHz range but decreases with frequency, leading to excessive insertion losses at the IF frequency (175MHz) [3]. Such a filter would have had higher losses than were allowed. Both IF filters are of 2-pole Tchebyscheff type, and using a combination of SMDs, integrated capacitors and integrated resistors, the performance is borderline. However, keeping the IF filters inside the MCM has the advantage of less noisy signals since the long lines going out and in the MCM are suppressed.

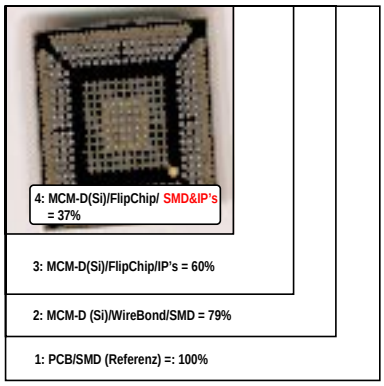

Figure 3. Area consumed by the different build-ups

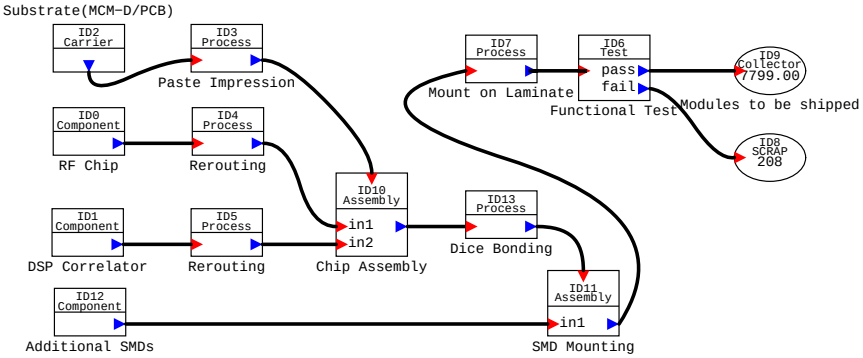

Figure 4. Generic MOE model of the different implementations

$$Final\ Cost_{ShippedUnit} = \frac{\Sigma Direct\ Cost_{Unit} + \Sigma_{all\ steps} Cost_{SCRAP} + \Sigma NRE}{No.\ shipped\ Units}. \quad (1)$$

Thus, solution 1 and 2 are ranked 100% (completely fulfilling the specs), whereas solution 4 gets 70% due to the lower safety margin) and solution 3 only 45% with a very narrow margin (percentages are derived from the relation of specified losses to calculated losses).

4.2 Area calculation

In Tab. 1 the area-relevant data for the different implementations are listed. The area required is calculated by the sum of the single components and performing a trivial placement. The results and rankings of the area comparison can be found in Fig. 3.

Solution 2 uses the well-known standard MCM-D technology with high yield (favorable in terms of cost), but requiring more area for wire bonding the dies (see Tab. 1) compared to flip chip mounting. The other two solutions spare substrate area using a substrate with integrated passives. The Si substrate was then mounted onto a laminate BGA package.

4.3 Cost calculations

Next to the direct material cost, yield aspects are also very important, since these values are very different for the various build-ups, as can be seen from Tab. 2. The respective substrate/board area calculated in the last section was fed into the cost modeling step to derive the overall implementation cost. Depending on the cost per area, the substrate cost can be deduced. Here, the trade-off problem becomes obvious: solution 3 can spare the entire assembly step for SMD components, but requires more substrate area due to integration of decoupling capacitors compared to solution 4.

The final cost is calculated using the general formula in Eq. 1. For this step we used the Modular Optimization Environment MOE, a cost modeling tool developed at ETH [8]. MOE maps the figures from Tab. 2 to a production model and routes the single components through this virtual production (see Fig. 4). Yield figures are translated into faults using Monte Carlo simulation. The routed components are inspected at the test steps and routed to the respective branch. With this tool, it is very easy to calculate the final cost including yield loss for the different implementations.

Fig. 5 presents the results of the cost analysis using the MOE tool. Setting the PCB cost to 100% and comparing the results for different cost and yield implications, we obtained a cost penalty of 4.7% (solution 2), 12.8% (solution 3), and 5.3% (solution 4). The cost penalty of solution 2 is caused by the higher substrate cost and the yield loss due to the (cheaper) not fully tested chips. For solution 3, eliminating the wire bonding reduces the yield loss significantly, but the large area required for especially the decaps raises the direct cost. Solution 4 has slightly lower direct cost than solution 2, but this is overcompensated by the higher yield loss.

4.4 Making a decision

For the final Figure of Merit, we calculate the product of the single factors in Fig. 6 (for more complicated cases weighting factors can also be introduced). The less area and the less cost, the better, therefore the reciprocal values are used. For solution 4, the “passives optimized” solution, we have a trade-off between the smallest form factor of all solutions (reduction to 37%), and a moderate cost penalty of 5.3% (compared to solution 1), resulting in the highest value

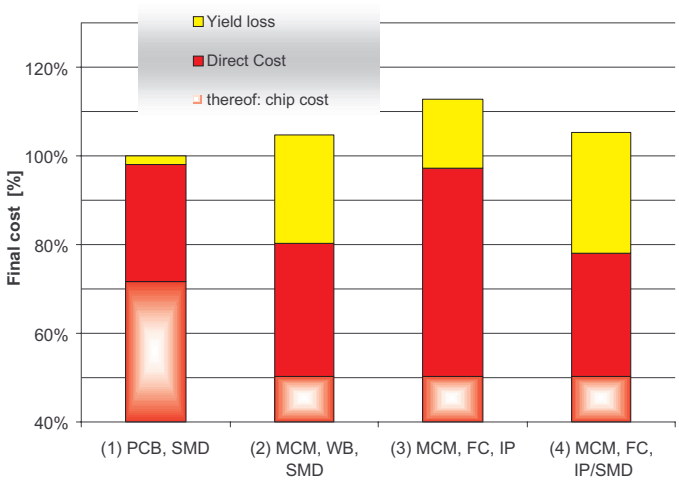

Figure 5. Cost analysis results using the MOE tool

	Perf.	Size	Cost	Π
(1)	1	1/1	1/1	1
(2)	1	1/0.79	1/1.05	1.2
(3)	0.45	1/0.6	1/1.13	0.66
(4)	0.7	1/0.37	1/1.06	**1.8**

Figure 6. Deriving the Figure of Merit

of 1.8. Solution 2 is slightly better than the PCB reference, whereas the full IP implementation suffers very hard from the performance penalty.

Therefore, an adaptation of solution 4 has been chosen for the final design. The silicon area of the final layout corresponded well with the predicted value for solution 4.

5 Conclusion

In this paper we presented a methodology to assess the use of integrated passves for a dedicated application. Taking our example of the GPS demonstrator, it has been shown that the impact of different technical solutions is not so easy to determine. Here, our methodology combining performance, size, and cost helps to derive a single figure of merit, serving as a basis for a design decision.

We demonstrated that especially for RF applications with a large amount of SMD components required, the use of integrated passives can pay off, however the combination of integrated and SMD passives should be evaluated as well. Thus, an even smaller form factor can be achieved by avoiding large-area-consuming integrated capacitors. Moreover, if the integrated solution does not provide the quality needed, using high-precision SMD filter components will not risk compromising the overall technical specifications.

Acknowledgment

Part of this work has been funded by the Swiss Government, Federal Office for Education and Science (BBW), under project 96.0117. The authors want to thank their colleagues from the EU research project SUMMIT, especially Michel Menard and Emmanuel Chataigner from THOMSON-CSF DETEXIS for their helpful comments and cooperation.

References

[1] Esprit Project 20492: Silicon Substrate Multi Chip Modules For Innovative Products. http://www.ife.ee.ethz.ch/mcm/summit/.

[2] H. Bleiweiss and E. Roelants. The Innovative SIMOV Technology. *Future Circuits International*, 4:153–159, 1998.

[3] J. Hartung. High Q Inductors for MCM-Si Technology. In *Proc. Int. Conf. on Multi-Chip Modules and High-Density Packages MCM'98, Denver CO, USA*, pages 256–261, 1998.

[4] T. Lenihan, L. Schaper, Y. Shi, G. Morcan, and K. Fairchild. Embedded Thin-Film Resistors, Capacitors, and Inductors in Flexible Polyimide Films. In *Proc. Int. Electronics Packaging Symp. IEPS'96, Austin TX, USA*, pages 192–202, 1996.

[5] C.-M. Lin, E. Logan, and D. Tuckerman. Precision Embedded Thin-Film Resistors for Multichip Modules (MCM-D). In *Proc. IEEE Conf. on Multichip Modules MCMC'97, Santa Cruz CA, USA*, pages 44–49, 1997.

[6] H. Pohjonen and E. Kuisma. Future Challenges for Passive Components in Wireless Communications Products. In *Proc. Wireless Communications Conf. WCC'96, Boulder CO, USA*, pages 31–32, 1996.

[7] C. Power, M. Realff, and S. Bhattacharya. A Decision Tool for Design of Manufacturing Systems for Integrated Passive Substrates. In *Proc. IMAPS ATW Integrated Passives, Denver CO, USA*, 1999.

[8] M. Scheffler, D. Ammann, A. Thiel, C. Habiger, and G. Tröster. Modeling and Optimizing the Cost of Electronic Systems. *IEEE Design + Test of Computers*, 15(3):20–26, 1998.