Welcome !

to the

Seminar

High Density Packaging

- Technologies and Applications -

Agenda

- **Presentation of Art of Technology**
- Motivation
- Introduction to HDP/MCM technologies
  - Definition
  - Advantages
- Technology Overview
  - Assembly/Interconnection
  - Substrates
- Application examples
- Typical HDP Project Flow
- Questions & Answers
- Discussion of possible customer projects

Who is Art of Technology – Company Facts

- Total of 10 years experience in electronic system design and miniaturization.
- Has its roots in the EU project EUROPRACTICE MCM (1995), whose purpose was to disseminate HDP/MCM technology in Europe.
- Company was founded in 1999.
- Successful project assignments in the
  - **Medical, Aerospace, Fixed and Wireless Communications, Sensor Technology, Industrial Computer …**
- Privately held company with strong partnerships.
- Winner of national and international awards.

EUROPRACTICE
MCM SERVICE

Art of Technology – Today

- Office and laboratory space at the Technopark Zurich

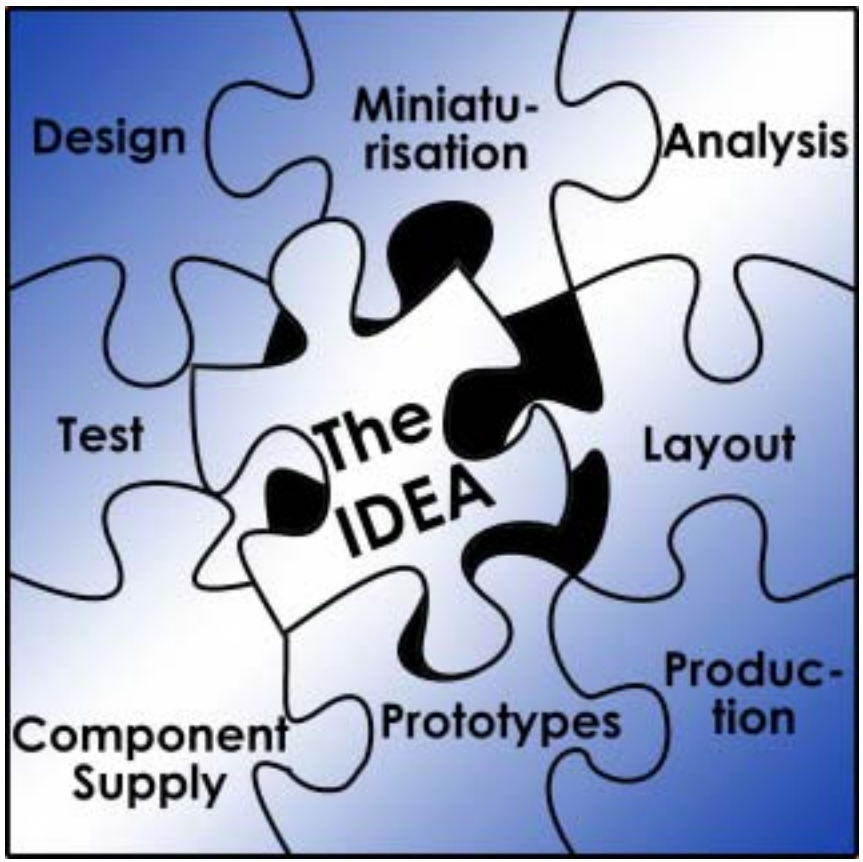
- Management system certified according to ISO9001:2000 and ISO 13485:2000
  (for medical applications, Certification according to ISO 13485:2003 planned for 2005)

- Core competences:
  - ✓Design excellence
  - ✓Miniaturization
  - ✓Customer specific solutions

The Services of Art of Technology

Turn-key electronic design and production,
or any part thereof together with customer engineering

- Development of ideas and solutions
- Basic research
- Concept studies & technology evaluation
- Miniaturization design
- System design incl. firmware
- Layout & production preparation
- Component procurement
- Evaluation of manufacturers and accompanying of the production
- Test & qualification



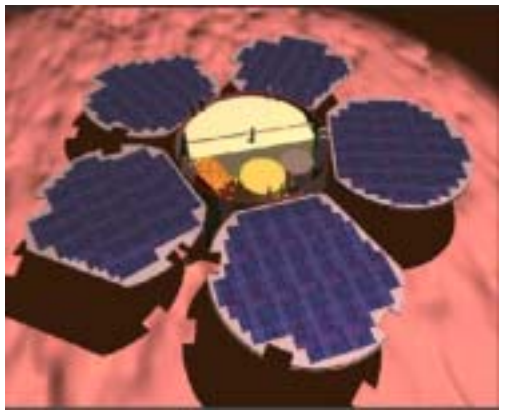
Art of Technology – Reference Projects

- **Aerospace/Packaging - Mars landing module, Contraves Space**
  - Feasibility Study for extreme environmental conditions
- **Medical/Miniaturization & System Design – AMON, Pendra**
  - System design including HW, SW, mechanics, DfM, DfT
- **Communications/HF - 2.5GHz antenna switch, Richard Hirschmann**
  - Fast turnaround HDP design instead of costly ASIC redesign
- **Research/Optics & FPGA**
  - Development of test platform for GHz E/O conversion module
- **Industrial/Sensors - ASAP**
  - HW/SW development of a low-power data logging sensor control unit
- **Medical/SW Development - Wearable Medical Devices (WMDs)**
  - CE/GAMP compliant FW development including risk management
- **Test/System Design – PCBs and devices**
  - Development of functional test stations for board and device tests

Reference Project – Aerospace/Packaging

Project:

Landing probes are being designed for a Mars mission. Art of Technology carried out a feasibility study as well as a technology evaluation of the electronics control legs for a measurement sphere and the measurement instruments.



Possible solution for the mars landing module

Main Challenges

- High vibration during take-off
- Storage at very low temperature during flight to Mars
- High shock when landing on Mars
- Wide temperature cycles during operation on Mars

AoT Solution

- Concept for Mixed assembly:
  - **SMD for small components**
  - **COB for large ICs**

Major Advantages

- Size and weight reduction
- Increase of reliability through:
  - minimization of stress on components and interconnections
  - minimization of sensibility to vibration and shock

Reference Project – Medical/Miniaturization

Project

Medical monitoring application with a novel sensor concept, which supplements blood glucose meters and helps to detect patterns and tracks in glucose levels

Device fits into a wrist-wearable ergonomically formed housing

Major challenges

Size, weight, power consumption, new measurement technology, stringent regulatory issues

AoT Solutions:

HW development (2 protos, 2 preseries, volume) using different levels of SMT vs. COB to reduce electronics volume step-by-step

From first concept idea to CE approval in 2.5 yrs!

Reference Project – Medical/System design

EU-Project AMON (Advanced Care & Alert Telemedical Monitor)

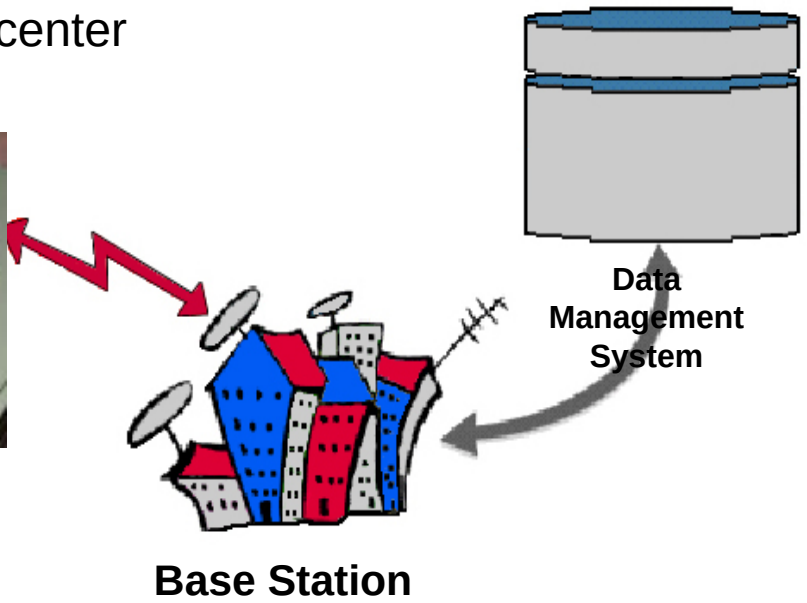
Project:

Wrist Wearable Medical Device for heart patients

Communication interface to telemedicine center

Variables Measured:

Temperature
Pulse
ECG
Blood Pressure
Blood O2



Special Features:

Emergency Button
GSM phone

AoT Solution:

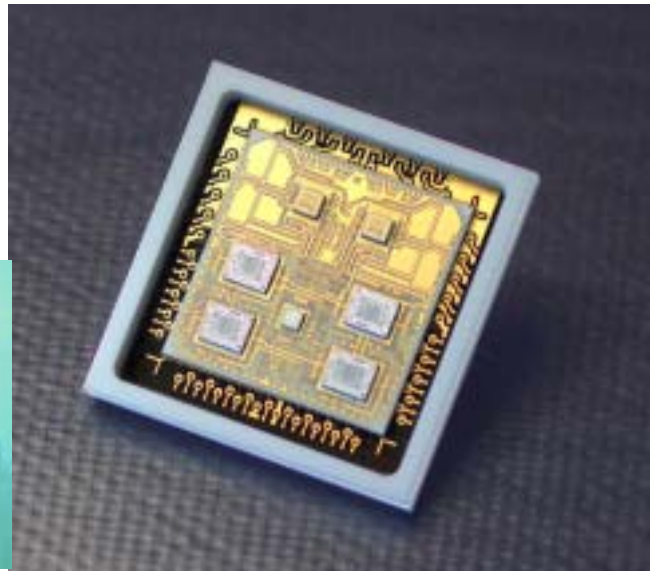
HW development, system design, overall packaging and testing

Project is winner of IST prize 2003!

Reference Project – Communications/HF

Project

9/4 Switch for 2.5GHz DB-Satellite-Signals based on an existing 5/4 ASIC, Hirschmann Electronics



AoT Solution 1 (1999)

– Technology Prototype: Thin film on ceramic

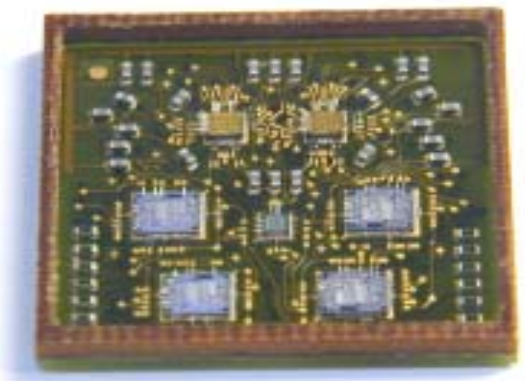
AoT Solution 2 (2001)

– Commercial version: SBU-Laminate

– No ASIC redesign

– 6 months turnkey

– Increased functionality



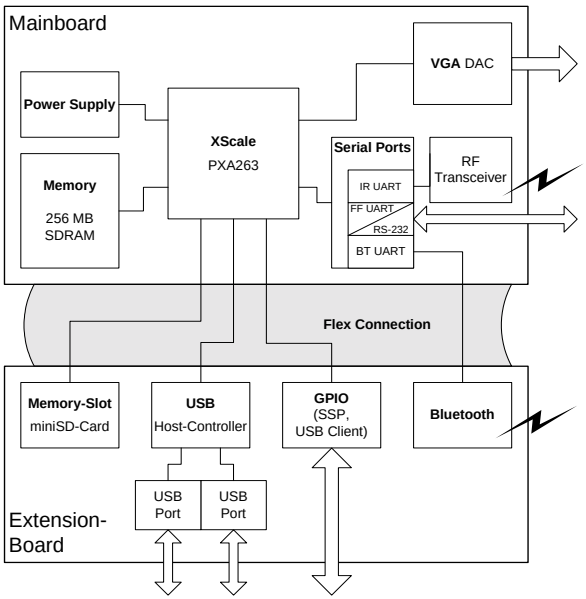
Kickoff to production within 6months, no ASIC redesign!

ART OF TECHNOLOGY

Reference Project – Computing/HW design

Project: QBIC Belt Integrated Computer

Wearable Computing Lab.
ETH Zürich



Key Features

- Low Power
- Small Size
- Flex Connection
- Standard Interfaces
  - USB, RS-232, RF, VGA, Bluetooth

AoT solution

- Fast turnaround first-time right prototype
- HW development
- Production support

Prototypes within 6 months, including component sourcing!

Reference Project – Industrial/Sensors

Project

- EU Project ASAP (Asset Surveillance And Protection
- System for container surveillance and localization
- Container localization with existing mobile communication infrastructure (not GPS), communication over the same infrastructure
- Successful installation of 6 sites in NL, successful alarm testing and propagation within 5min over several 100kms

Left: rugged onboard unit, **right**: bromide sensor installation

AoT Solution

- Sensors for different applications, s/a temperature for freezer container, gas sensors for bromide transports
- Autonomous control of sensors, communication to main system
- HW, FW development, prototype mechanics

Reference Project – Research/HW & SW FPGA

Project

- Test platform for electro-optical conversion module operating in GHz range

Major challenges

- HW/SW Codesign
- Clocking and LVDS routing
- Power budget

AoT Solutions:

- System & board design
- FPGA programming
- Prototype build up and test

Tools/platforms:

- Xilinx Virtex

Reference Project – Medical embedded SW

Project

Firmware for embedded, wearable medical device

Major challenges

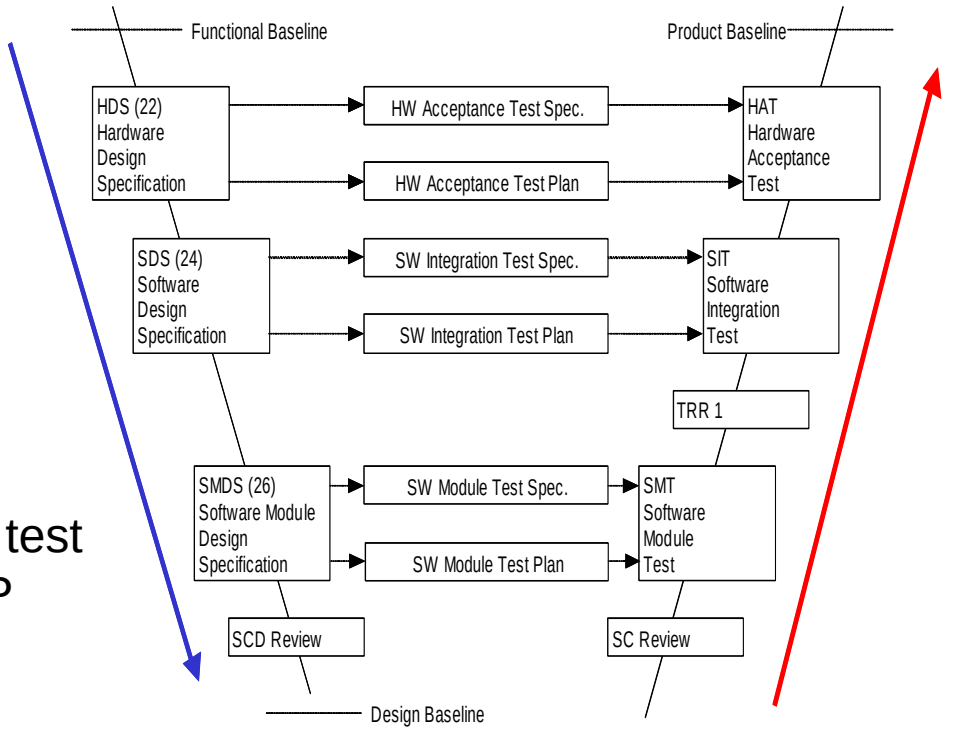
- Modular design
- High reliability
- Risk management

AoT Solutions:

- SW requirements specification
- SW design, implementation and test
- Documentation according GAMP

Tools/platforms:

- 8 bit µC, C, SW version control, AoT Quality System



Reference Project – Engineering Support SW

Project:

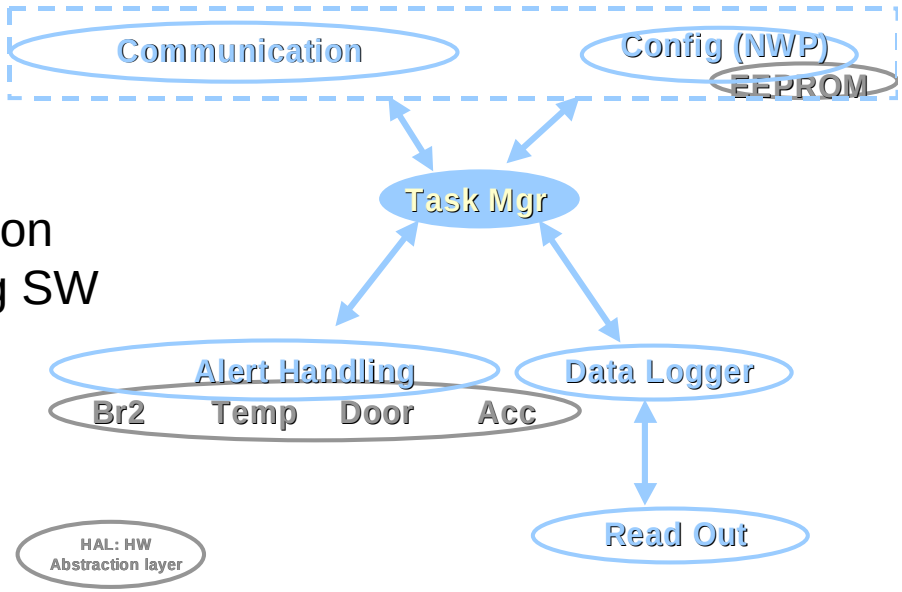
- Windows operated support SW

Major challenges

- Lean GAMP based SW development process
- Open communication protocol

AoT Solutions:

- WIN-driver for device communication
- Device configuration and operating SW
- Online database access for device data
- Data extraction for offline analysis
- System test



Tools/platforms:

- PC, C, C++, SW version control, AoT Quality System

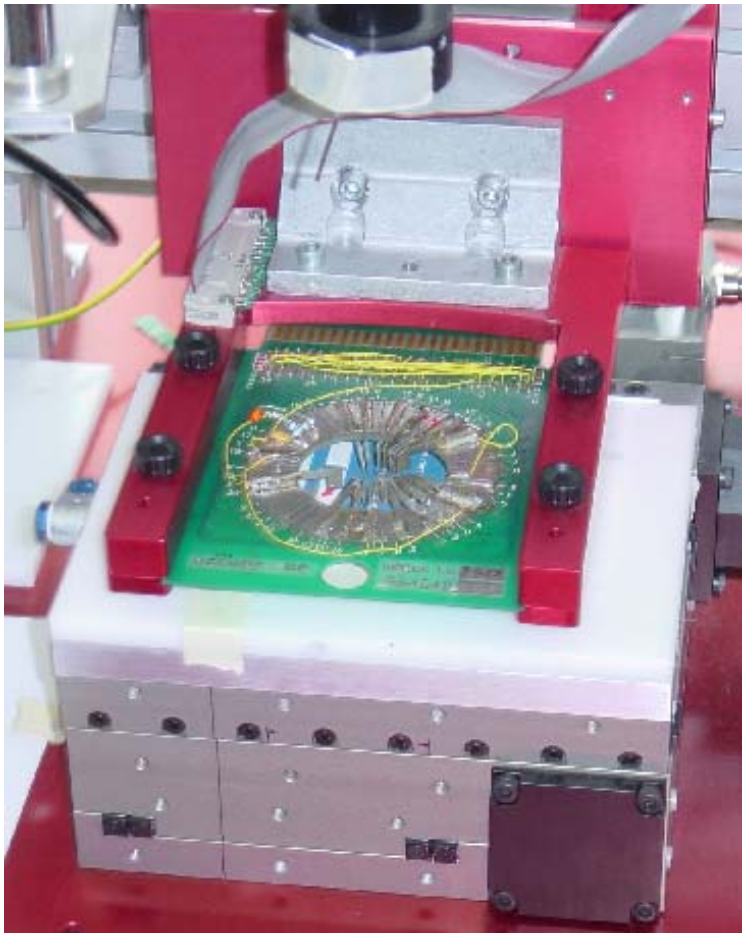
Reference Project – Test HW & SW

Project

Automated functional testing of medical devices requiring full traceability over lifecycle

Major challenges

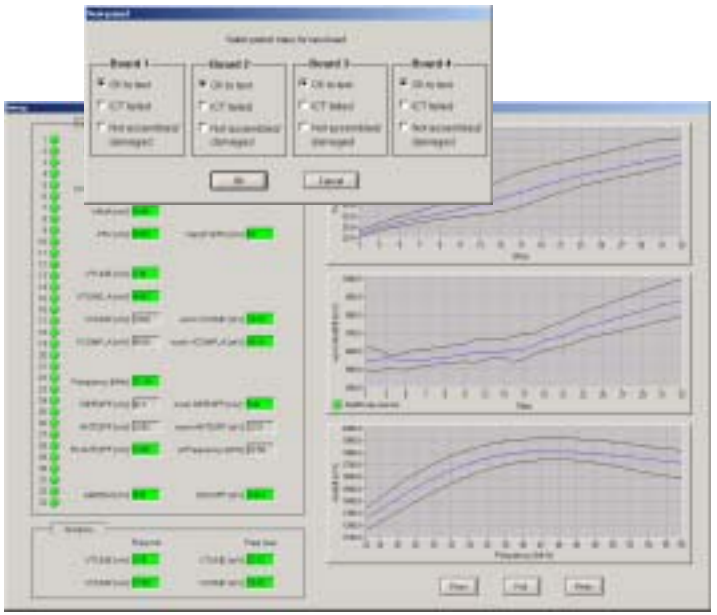
- Traceability till electronic module level
- Logging of all manufacturing and test steps
- Heterogeneous multi vendor environment
- Multi site installation for test and assembly
- Distributed database with remote access
- Multi level skilled operators



Reference Project – Test HW & SW

AoT Solutions:

- Design and implementation of DB system
- Database integration of multi vendor environment
- Connection to embedded medical device
- Visualization for test operator
- Online access for MS office applications
- Data export for offline analysis
- Support for production, repair, service
- Database synchronization



Tools/platforms:

- PC, custom HW, NI DAQ card, LabWindows, SW Version control, AoT Quality System
- MS-Access and MySQL Database

ART OF TECHNOLOGY

Competences: Design excellence

Proven design experience for analog and digital hardware and software for embedded systems

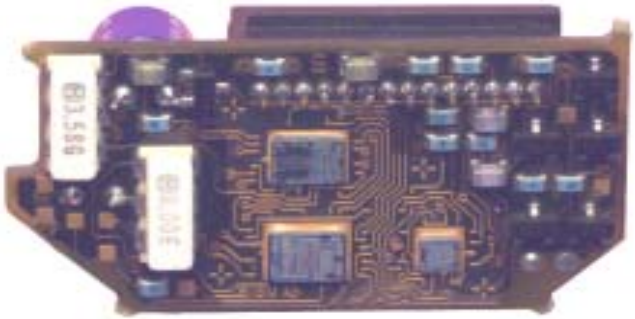
- Flexible and fast turnaround design and development
- Integrated development of hardware and related software
- Flexible and adaptable quality system ensures adequate quality level from first design step till production
- Quality system according to ISO 9001, ISO13485, GAMP

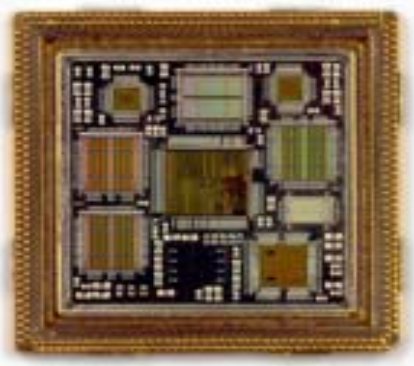
ART OF TECHNOLOGY

Compentences: Miniaturization Technologies

Miniaturization of electronic systems through High Density Packaging (HDP/MCM)

COB
Chip on Board





MCP
Multi Chip Package

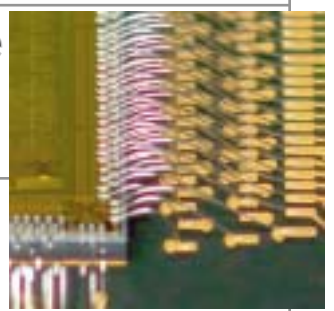
ART OF TECHNOLOGY

Competences: Customer specific solutions

Our speciality:

- use of technologies available on the market
- use of well established and reliable processes
- use of new combinations thereof to fulfill the customers systems special needs and requirements

System requirement	System	Solution
Package with high peripheral pincount not available on market	**Computer module**	Thin film on silicon substrate in a PSGA (plastic stud grid array) package (molded plastic, copper surface, laser structured)
Biomedical compatibility	**Biomedical sensor**	Gold on ceramic with thermo printer glass cover
Avoidance of extraordi-nary expensive BGA on ceramic	**Communication module**	Thin film on ceramic substrate on laminate carrier with BGA with plastic cover
Combination of very high pin IC and low cost substrate	**Computer module**	Wire Bonding 2 rows on IC to 3 rows on substrate



ART OF TECHNOLOGY

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Motivation

"Packaging is the bridge between fast moving semiconductors and slow moving PWBs and is becoming more important, complex and profitable as the gap increases."

Ken Gilleo; VP Technical Programs, Cookson Performance Solutions, USA; Editor of "Area Array Packaging Handbook, Manufacturing and Assembly"

"We are entering an arena that makes IC integration expensive and slow in turn around. The MCMs are therefore required as we face IC integration issues particularly with heterogeneous or diverse set of chips."

"HDP/MCM is required in the future because of IC integration issues and higher I/O chips. You are limited by smallest components with finest pitch –both are difficult to achieve beyond where we are or will be shortly. So MCM/HDP is the only way to go for those products that require either high electrical performance or smaller form factor or both."

Rao Tummala; Chair Professor Georgia Institute of Technology in Microsystems Packaging; President of IEEE-CPMT Society; Introduced ceramic MCM technology to the industry in 1982 whilst with IBM

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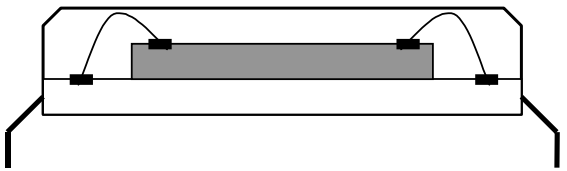
What is High-Density Packaging

- HDP/MCM is the next logical step towards miniaturised electronics
- Miniaturisation:
  - smaller than PCB/SMD
  - larger than ASIC



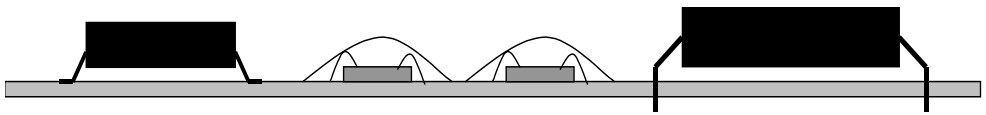
Single - Chip - Package

- Until now every single Chip has been packaged into a package (SCP) and was then assembled onto a PCB board (through hole, SMD)

What is High-Density Packaging

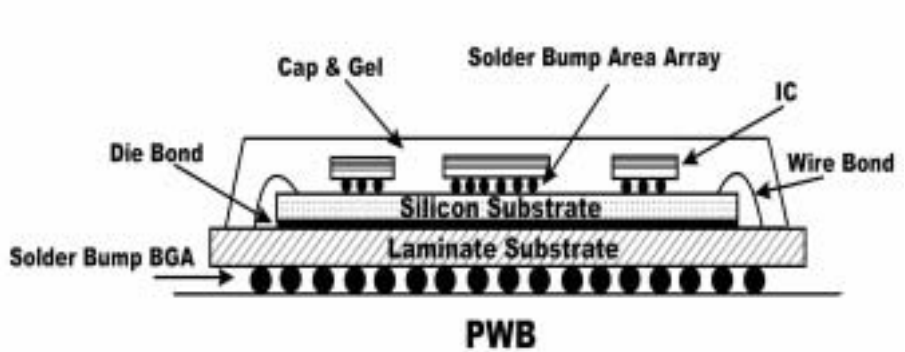
Now unpackaged Chips are used. They will be assembled

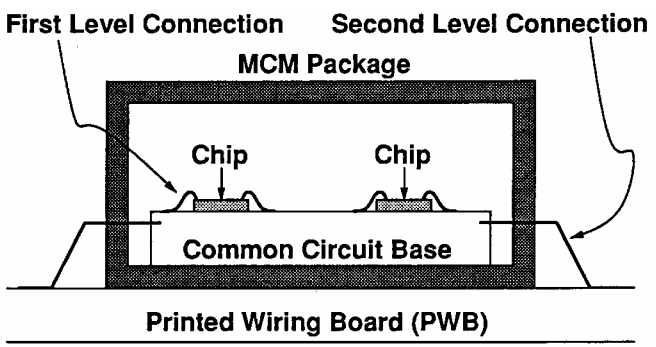
- either directy onto the PCB board (COB) or



Chip - on - Board

- several Chips together into a package (MCP) and then onto a board.



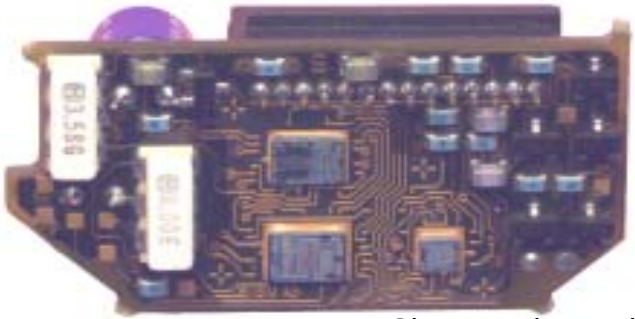


Multi - Chip - Package

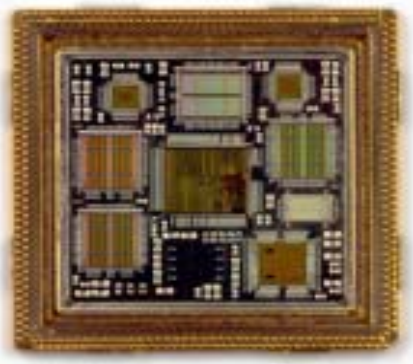
Example Miniaturization Technologies

Miniaturization of electronic systems through High Density Packaging (HDP/MCM)

COB
Chip on Board



Charger Electronics



1 cm

MCP
Multi Chip Package

What is High-Density Packaging

- HDP-Modules are built using
  - Bare Dies (unhoused chips)
  - µ-BGAs or other Chip Size Packages (CSPs)
  - Highly integrated circuit boards (substrate)
  - Different assembly technologies

- A HDP-Module is either complete system or part of a system
  - packaged in a PGA/BGA and then mounted onto a PCB

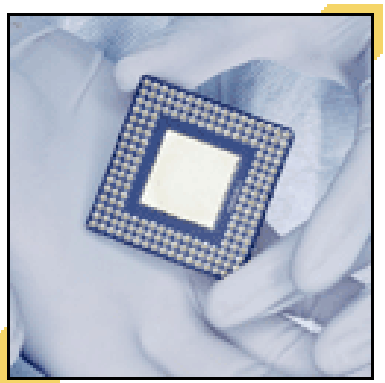
Advantages of HDP/MCM?

Advantages of the HDP/MCM-Technologies are:

- Shorter development times and overall faster time to market than an ASIC
- Easy combination of different technologies (µC, Power electronics, HF, memory, etc.)
- Increase of functionality while reducing size and weight
- Increased performance, reduced power consumption
- Easier protection against EMC and EMI
- High reliability
- Cost reduction at system level
- Increased modularity and reusability of subsystems

Where to use HDP/MCM?

HDP/MCM Application areas include



- All applications where many features need to be integrated into a small, lightweight, low-power – often mobile or wearable – device.
- Applications in mixed-signal electronic systems as an alternative to a costly, risky and time-consuming ASIC design.
- If you already have designed ASICs, HDP/MCM will allow you to efficiently and inexpensively use them to offer a wide range of product variations.
- Applications to be used under extreme environmental conditions such as temperature, electromagnetic interference etc.

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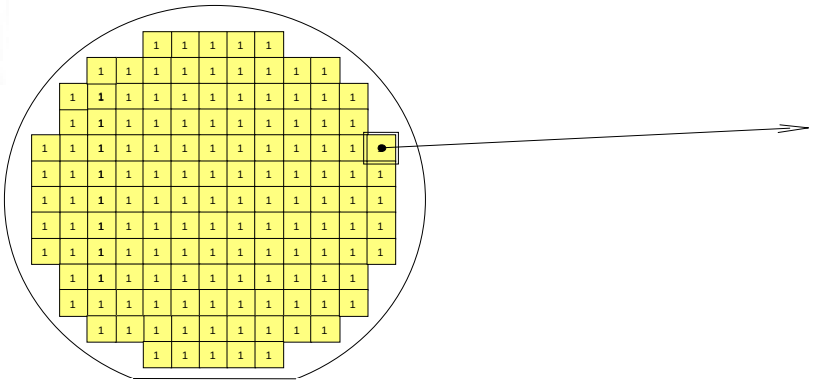
Assembly

What is inside a chip package:

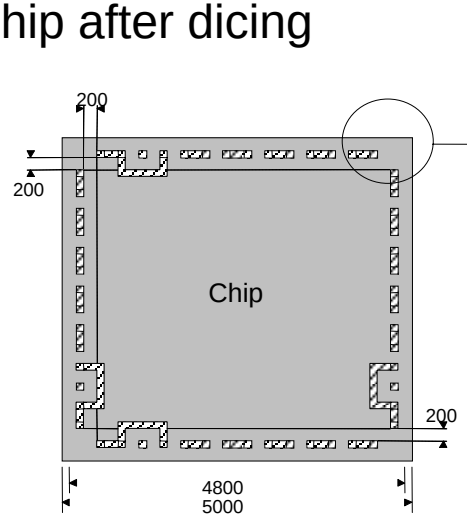
Assembly

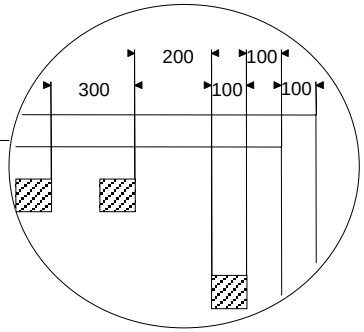
Si-Wafer

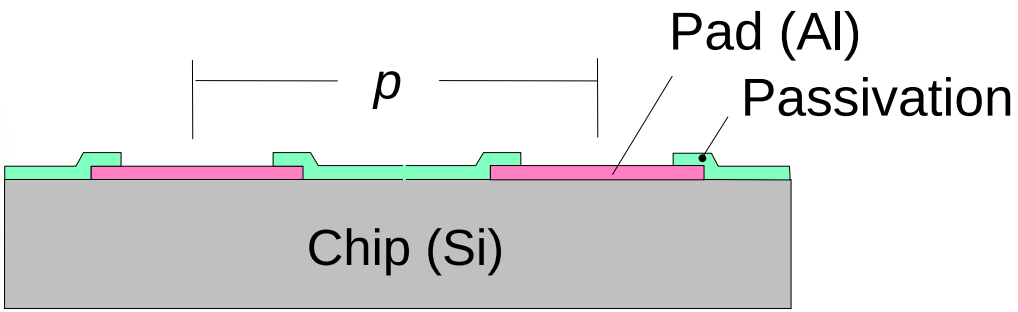
Diameter 4-12"



Chip after dicing







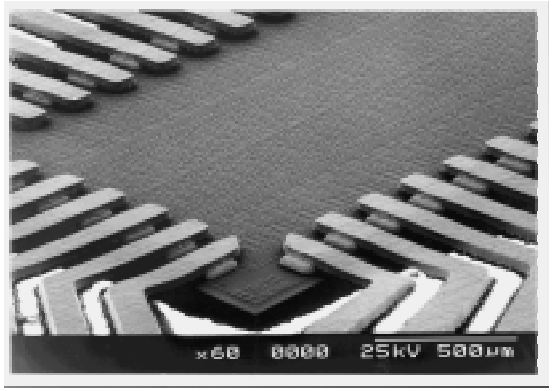
Important Data

- Chip Size, Thickness
- Pad Size
- Min. Pad Pitch *p*

(Pad center – Pad center)

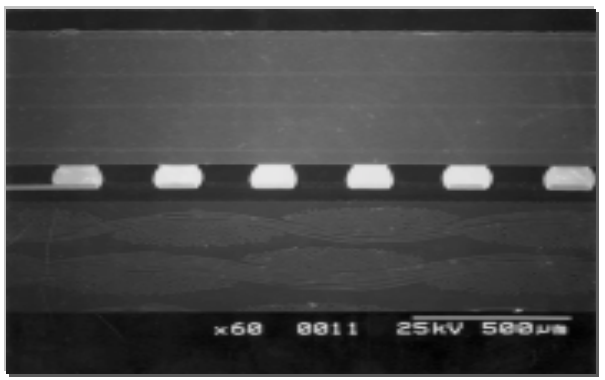
Assembly

Bonding-technologies:



Wire bonding

Tape **A**utomated **B**onding

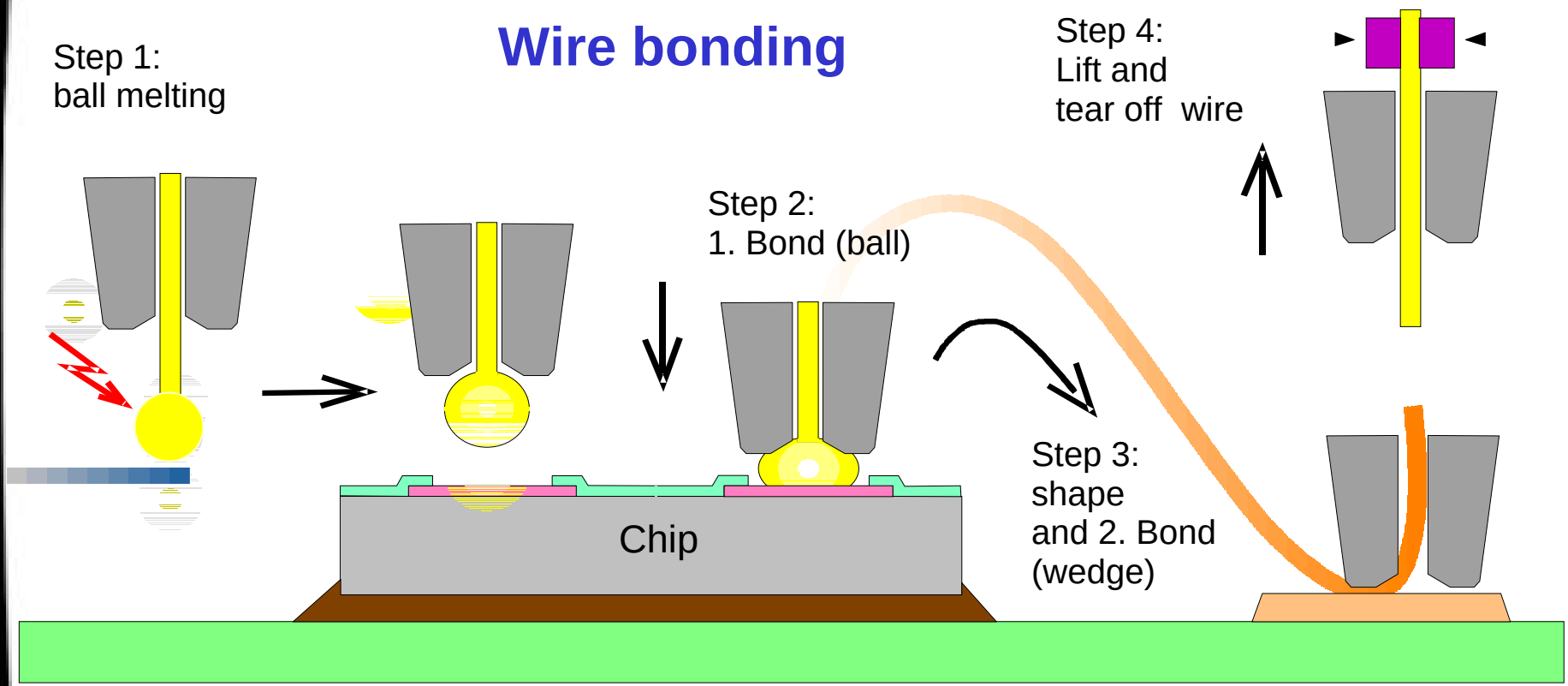


Flip Chip

ART OF TECHNOLOGY

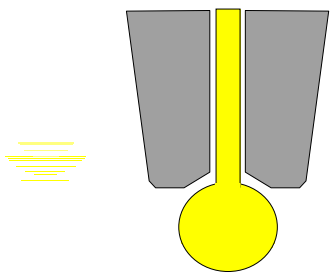
Assembly

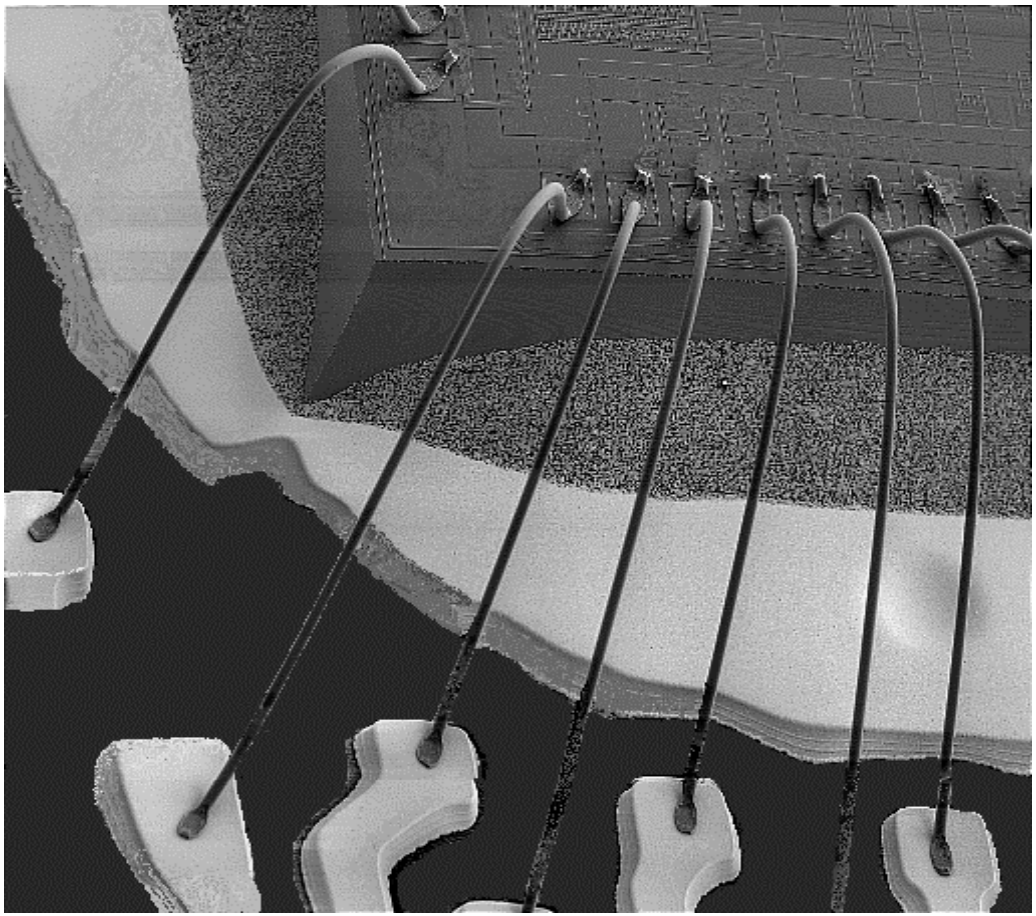
Wire bonding



Assembly

Wire bonding

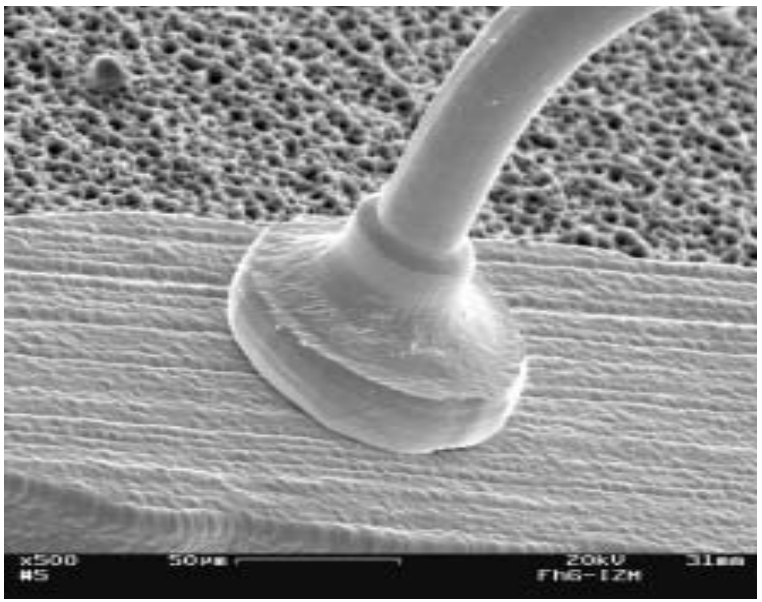




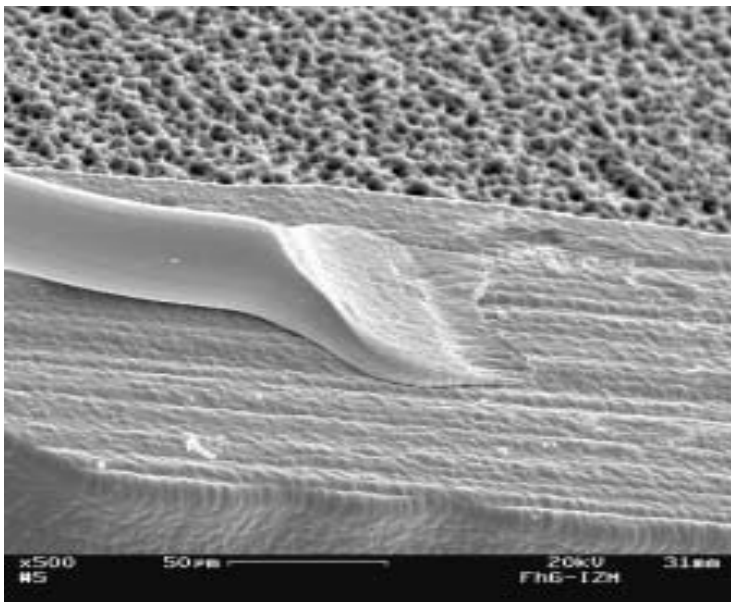
ART OF TECHNOLOGY

Assembly

Ball Bond



Wedge Bond



Assembly

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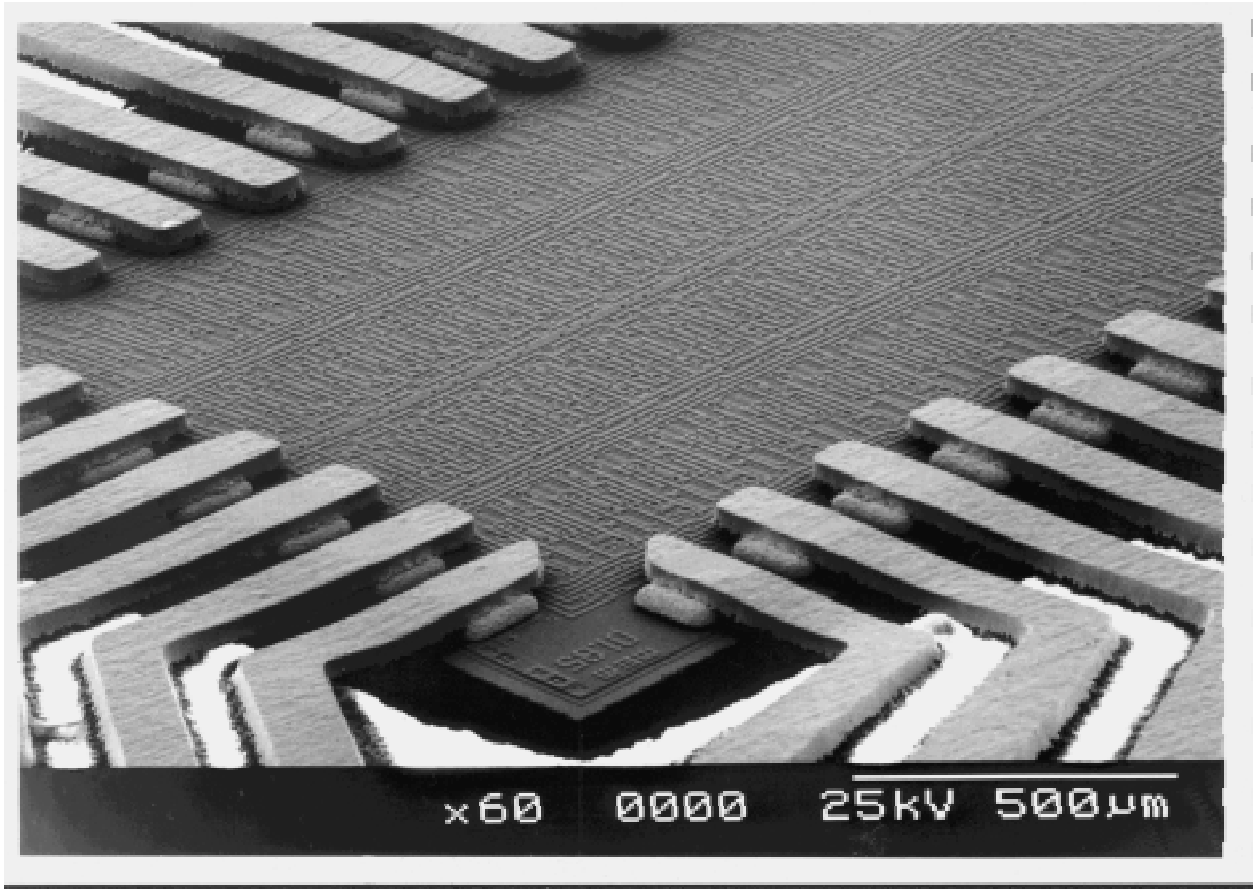
Tape Automated Bonding



Assembly

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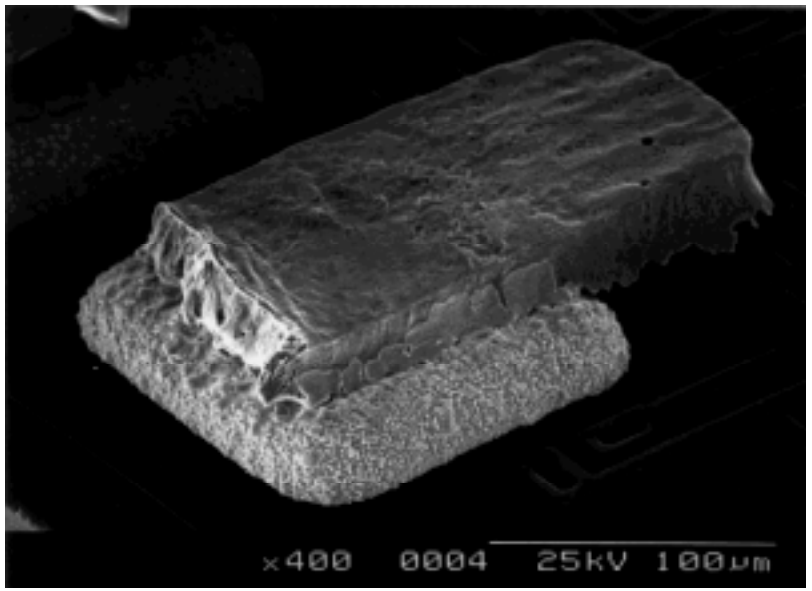
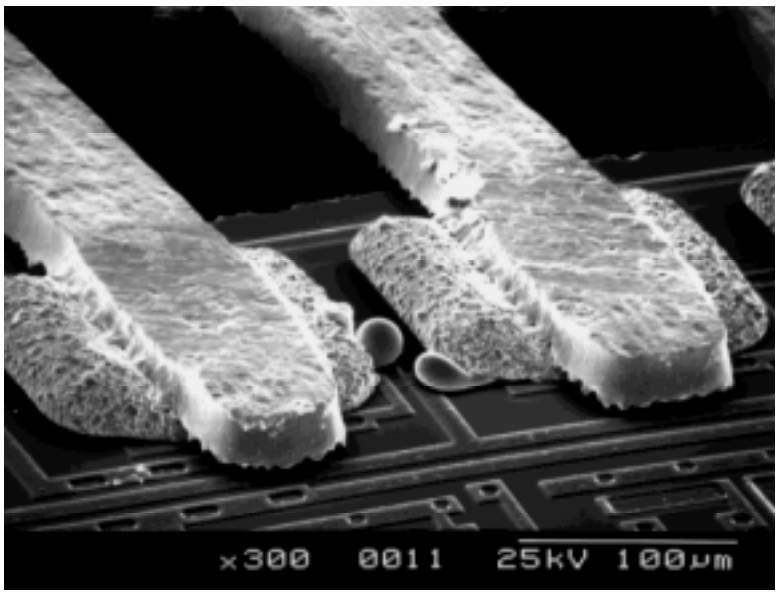
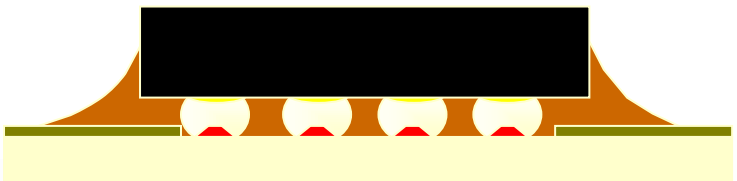


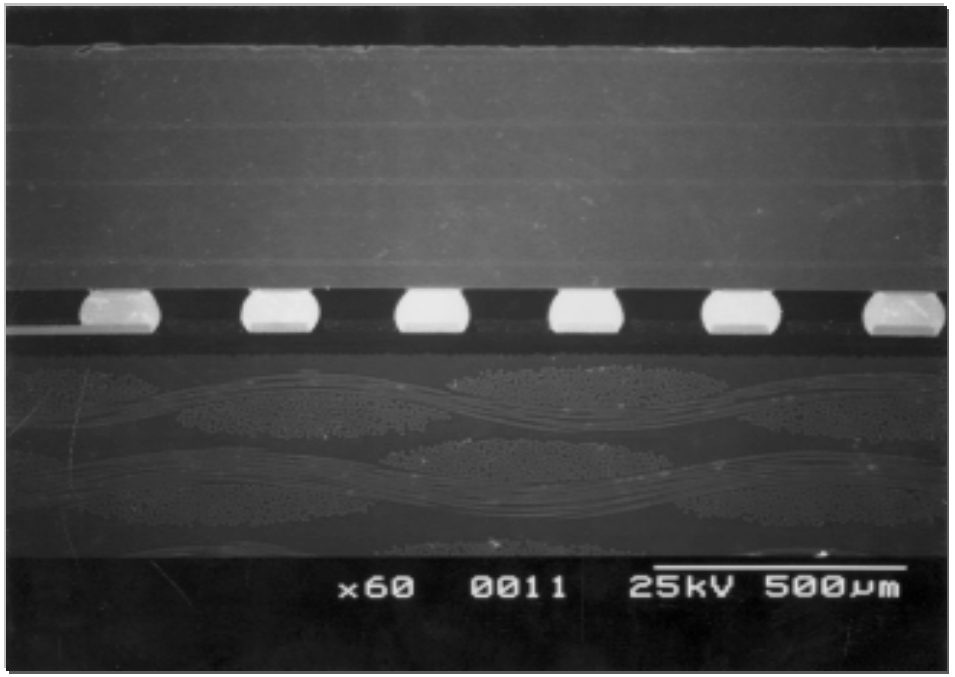


Assembly

Flip Chip

Direct Chip Attach

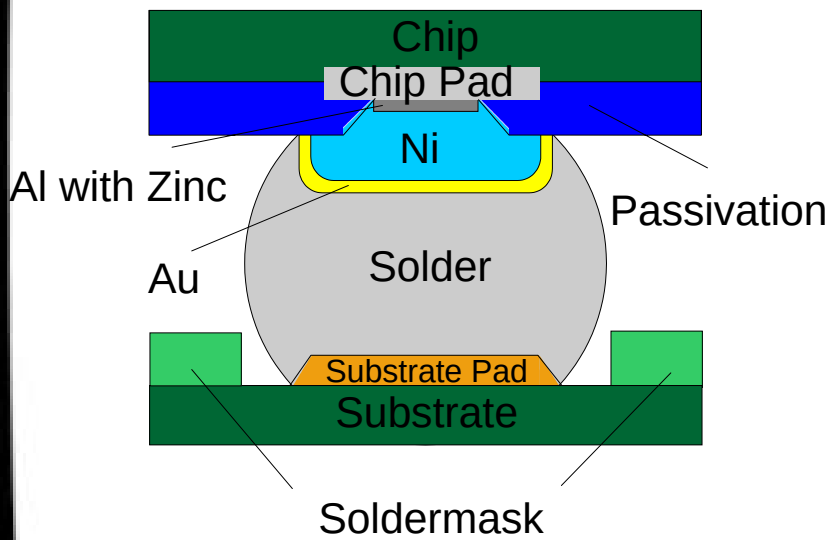


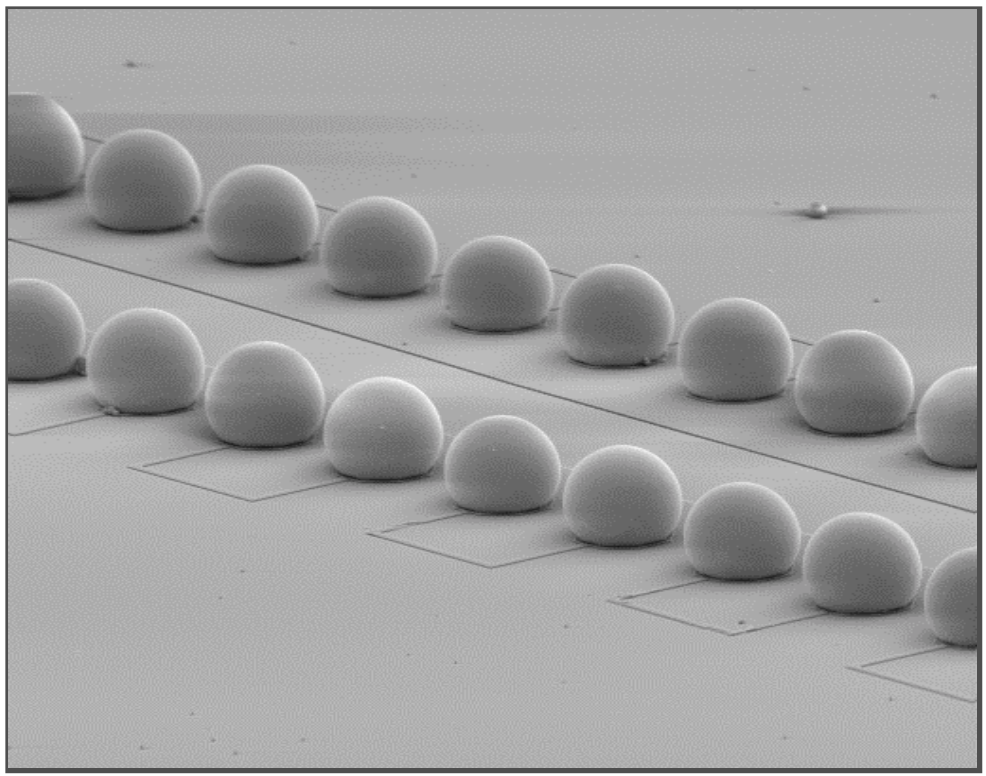


PITCH: 200 µm

Assembly

Flip Chip

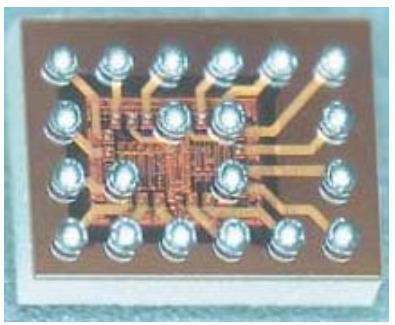




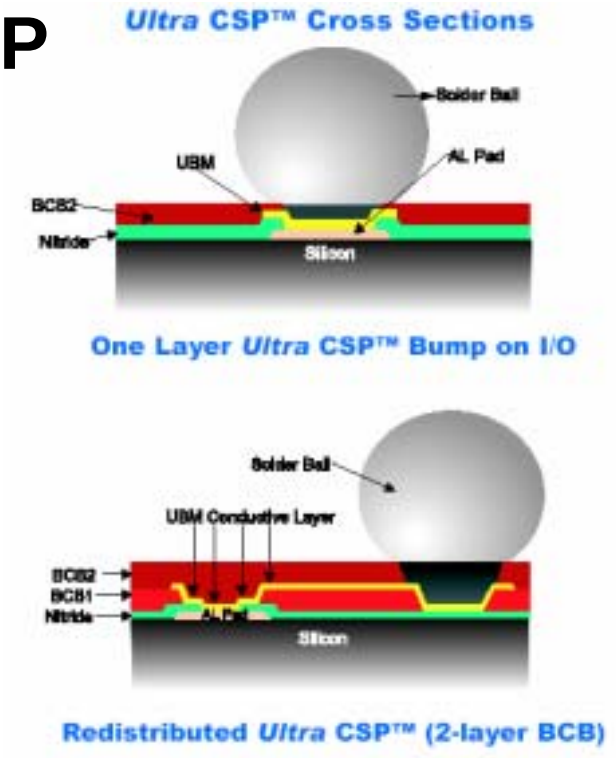
Assembly

Waver level packaging for CSP

- without redistribution of pads
- with redistribution of pads



Pictures: source FhG-IZM



Pictures: source AMKOR

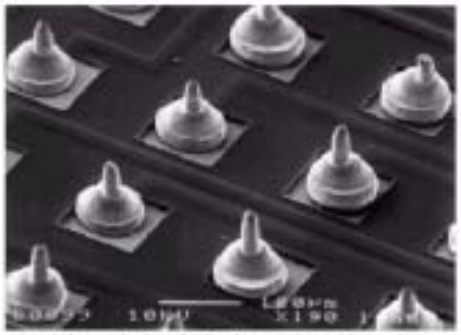
Die thickness	> 0.36mm
Bond pad pitch	> 40 µm
Redistribution Line	> 25 µm
Space	> 12 µm
Solder ball pitch	> 0.3 mm

Assembly

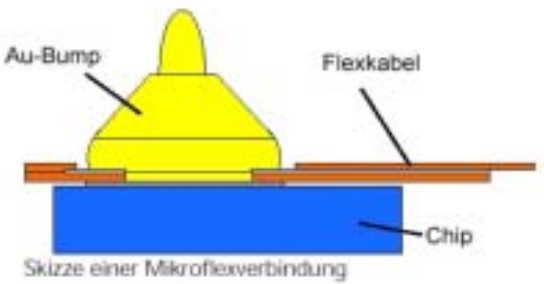
Special approaches to the Assembly technologies

- Micro-Flex connection (right)
- Chip-on-Chip (below)

Pictures: source Valtronic SA



Rasterelektronische Aufnahme eines Kontaktarrays



Skizze einer Mikroflexverbindung

Pictures: source FhG-IBMT

Assembly

PBGA

Family of new packages

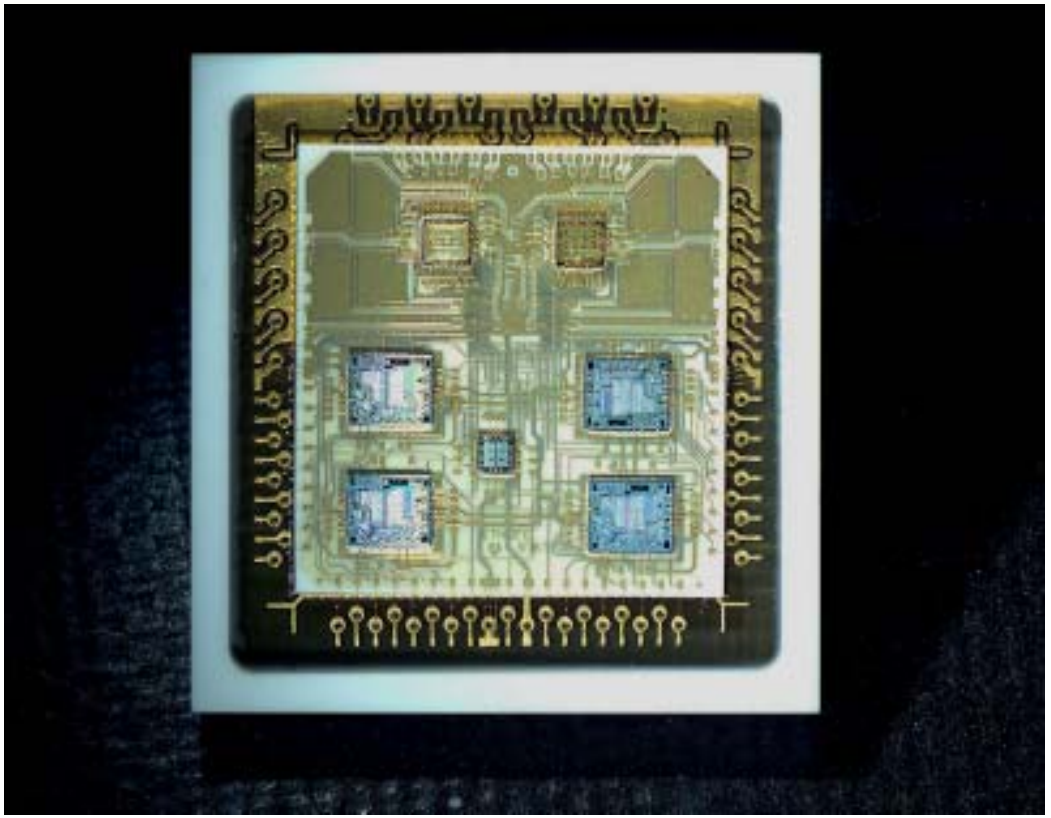
CSP (Chip Scale Package) with carrier

CSP (Chip Size Package) rerouting on chip

Flip Chip

Assembly

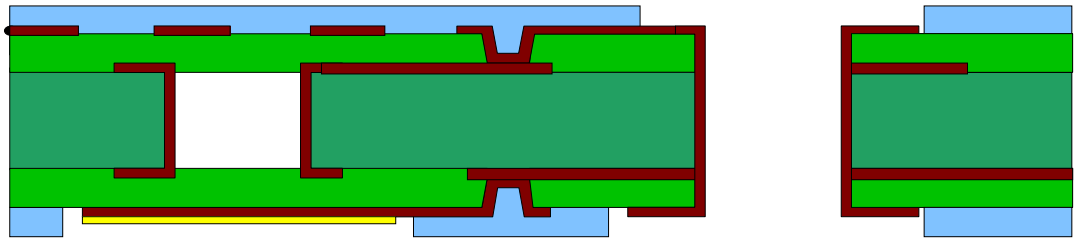
- The same technologies can be used to pack several chips into one package.
- Complete products can be built as such.
- For both applications new connection technologies are needed, which reach beyond the integration density of an ordinary circuit board.

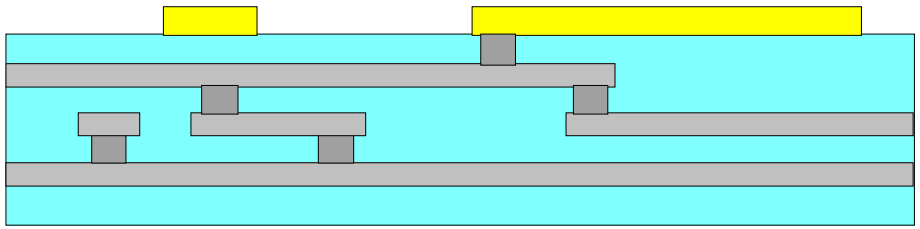


➡ **Substrate**

Substrate

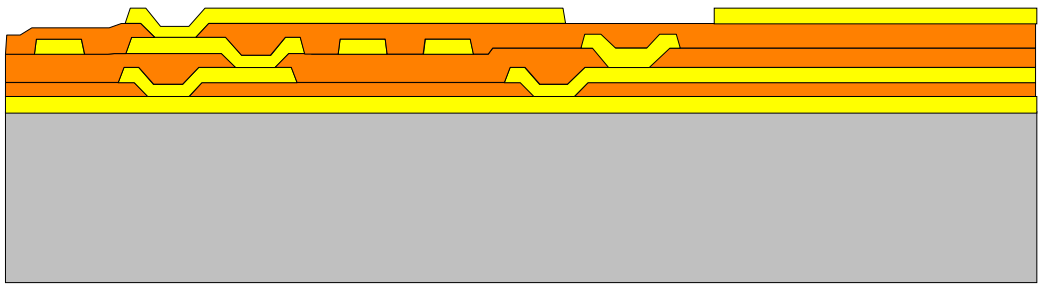
Laminate



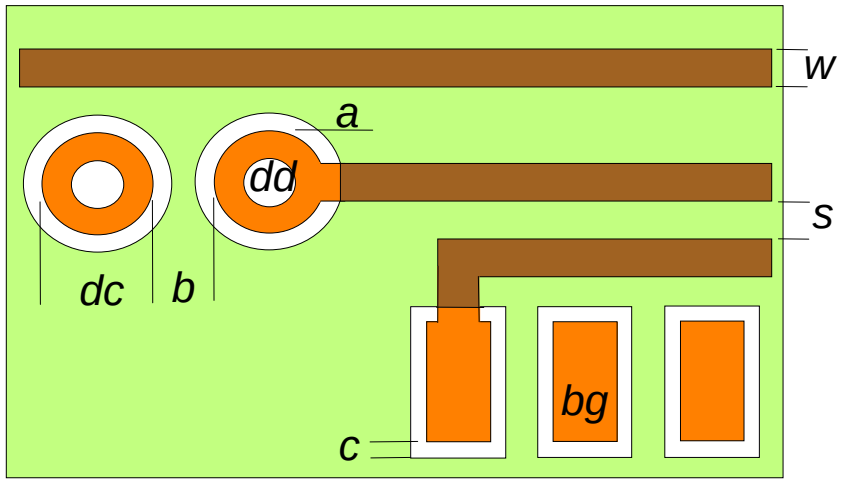


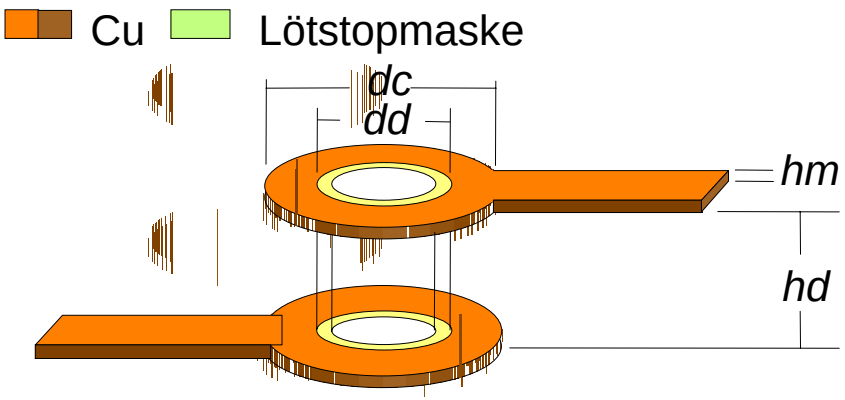
Ceramic

Thin film



Substrate



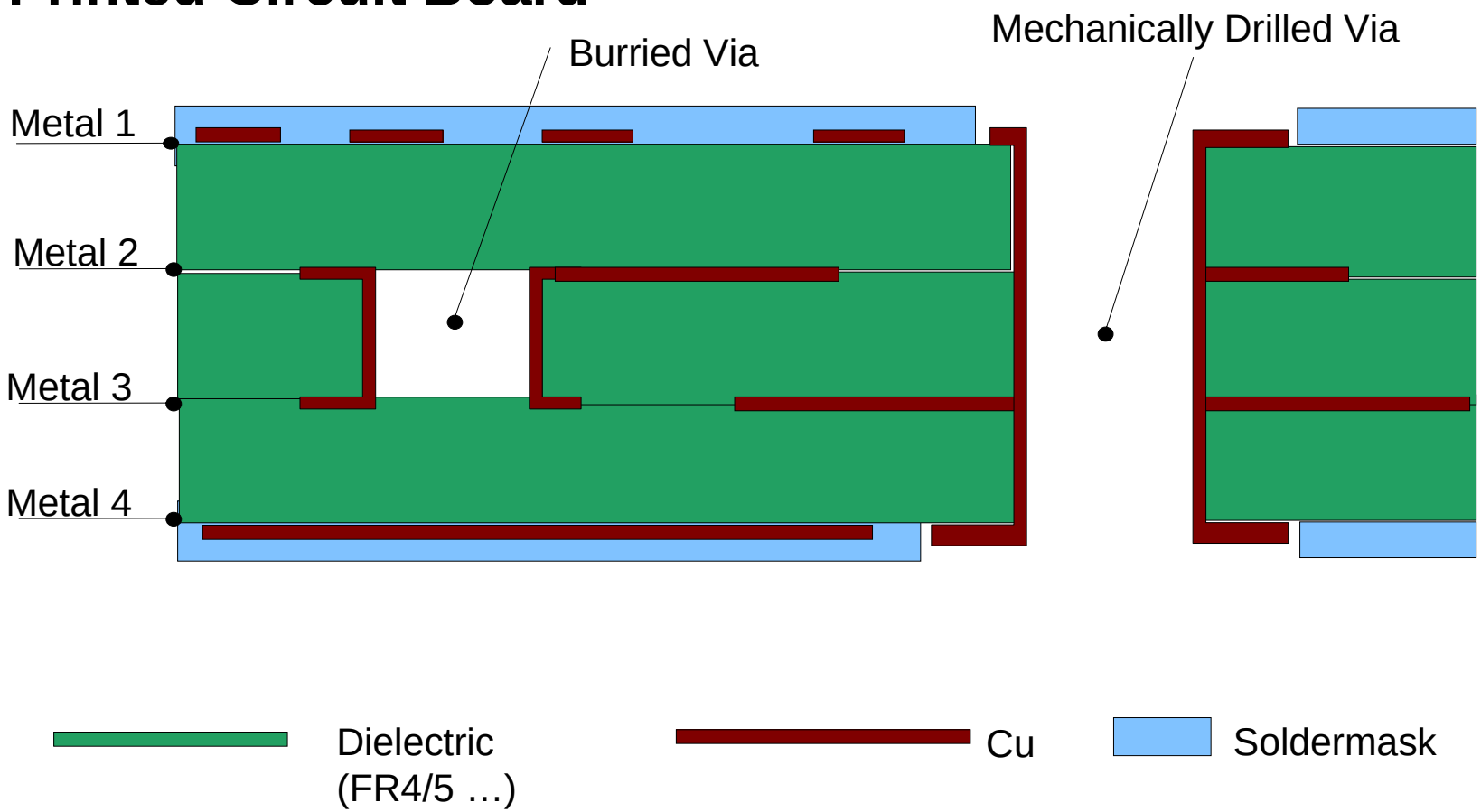


Substrate rules:

Line:	min. width	***w***
Via:	min. Pad diameter	***dc***
	min. Hole diameter	*dd*
Spacing	Line-line	***s***
	Line-Via *a*	
	Via-Via	*b*
Thicknesses	Metal	***hm***
	Dielectric	***hd***
other	Soldermask over width	*c*
	bond pad with	*bg*

Substrate

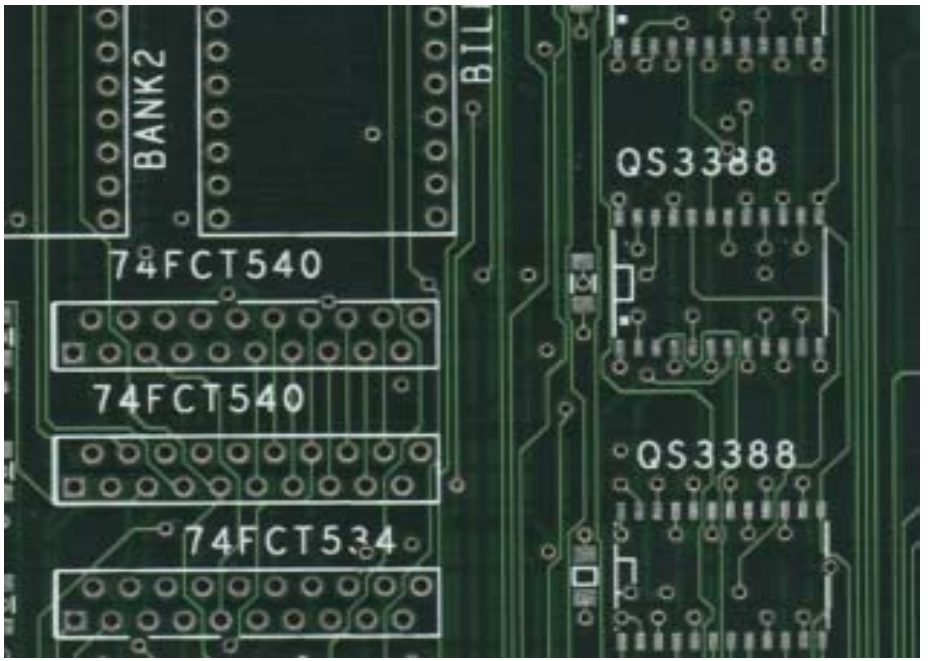
Printed Circuit Board



Substrate

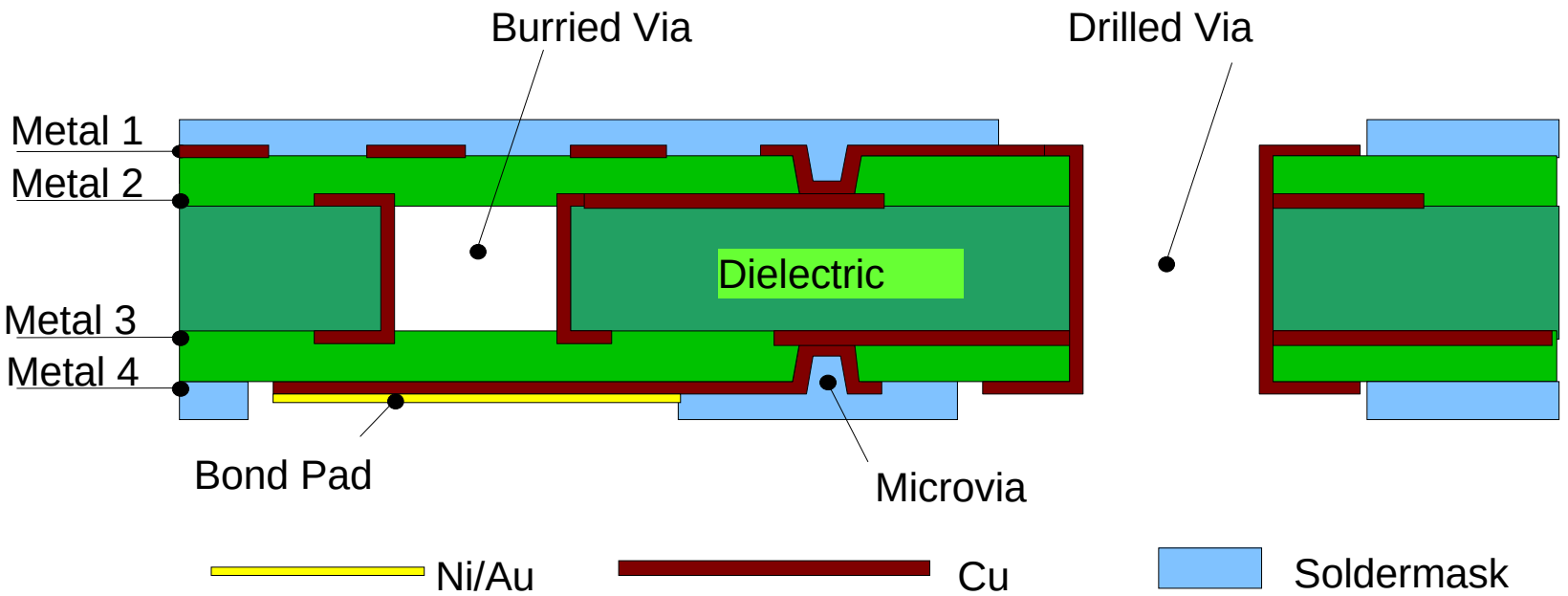
PCB

Line width/pitch	> 100 / 200 µm
Via pad diameter	> 500 µm
Number of layers	2-12
Dielectric thickness	100 - 1000 µm
Metal thickness	15 - 35 µm



Substrate

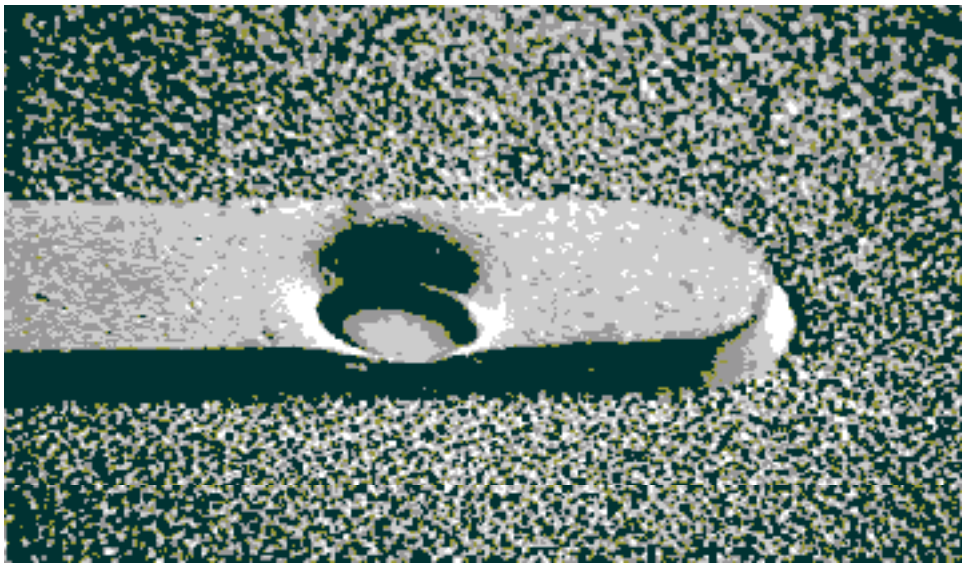
Sequential Build-Up (SBU)
Microvia vs Mechanical Drilling



Substrate

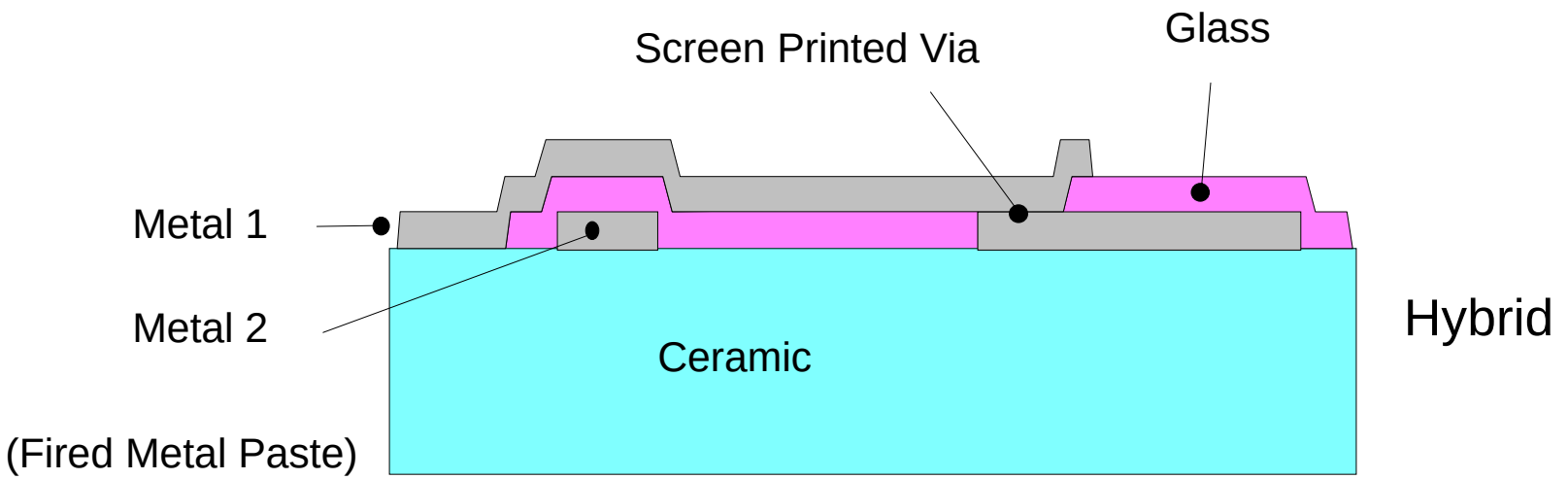
SBU/Microvia

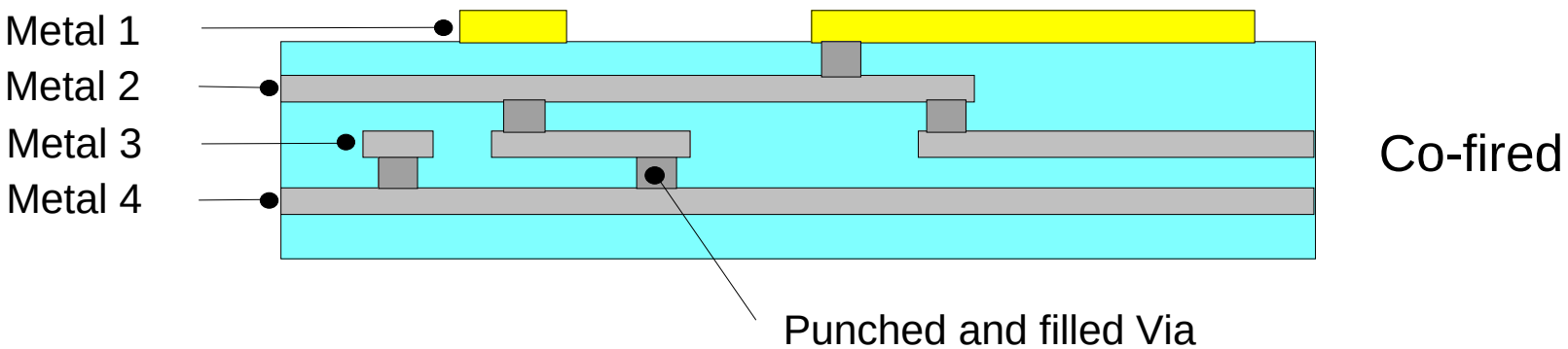
Line width/pitch	> 50 / 100 µm
Via pad diameter	> 250 µm
Number of layers	2*3 + PCB
Dielectric thickness	25 - 100 µm
Metal thickness	10 - 35 µm
Via formation	Photochemical, Mechanical, Laser



Substrate

Ceramic

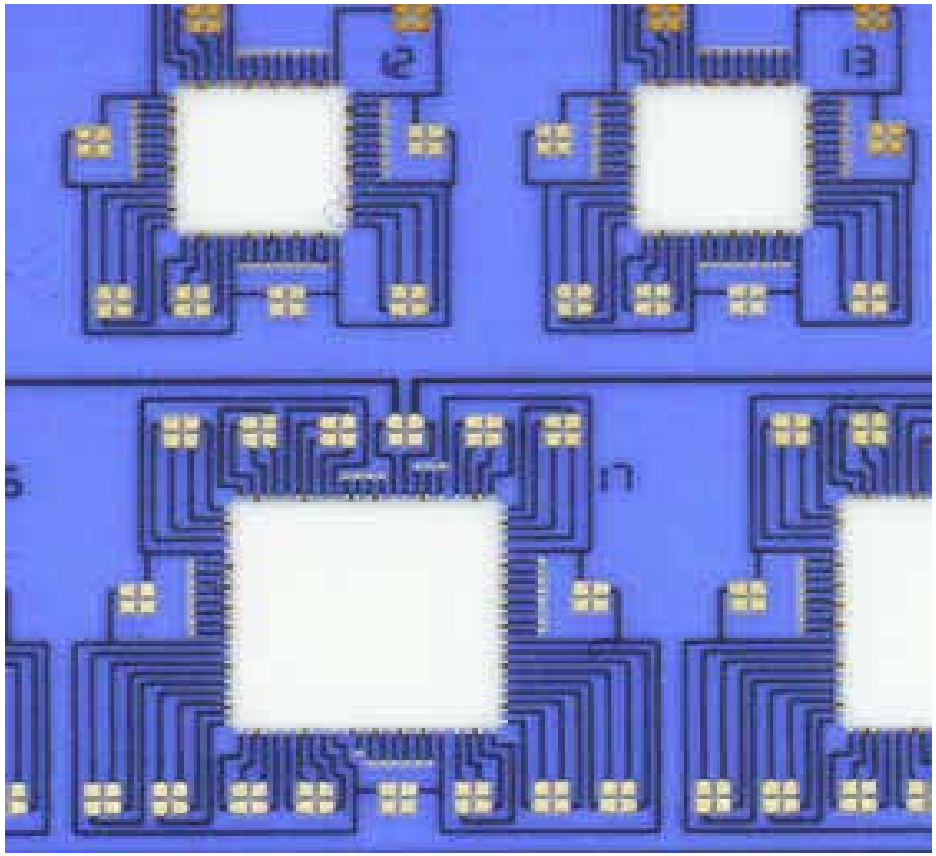




Substrate

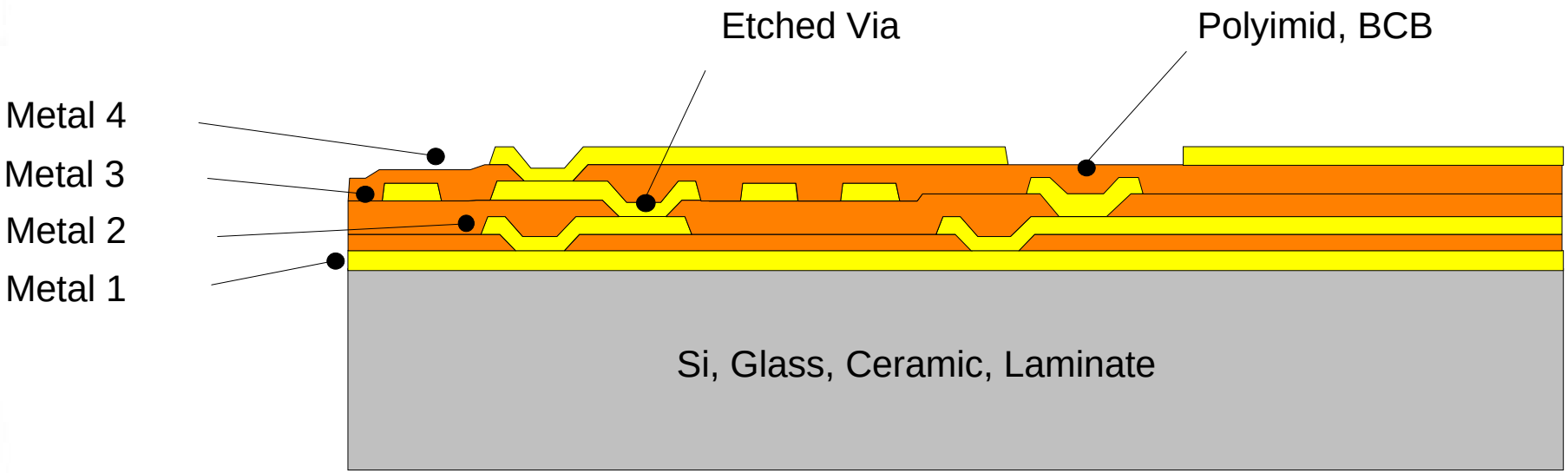
Ceramic

Line width/pitch	125 / 250 µm
Via pad diameter	> 200 µm
Number of layers	3-30



Substrate

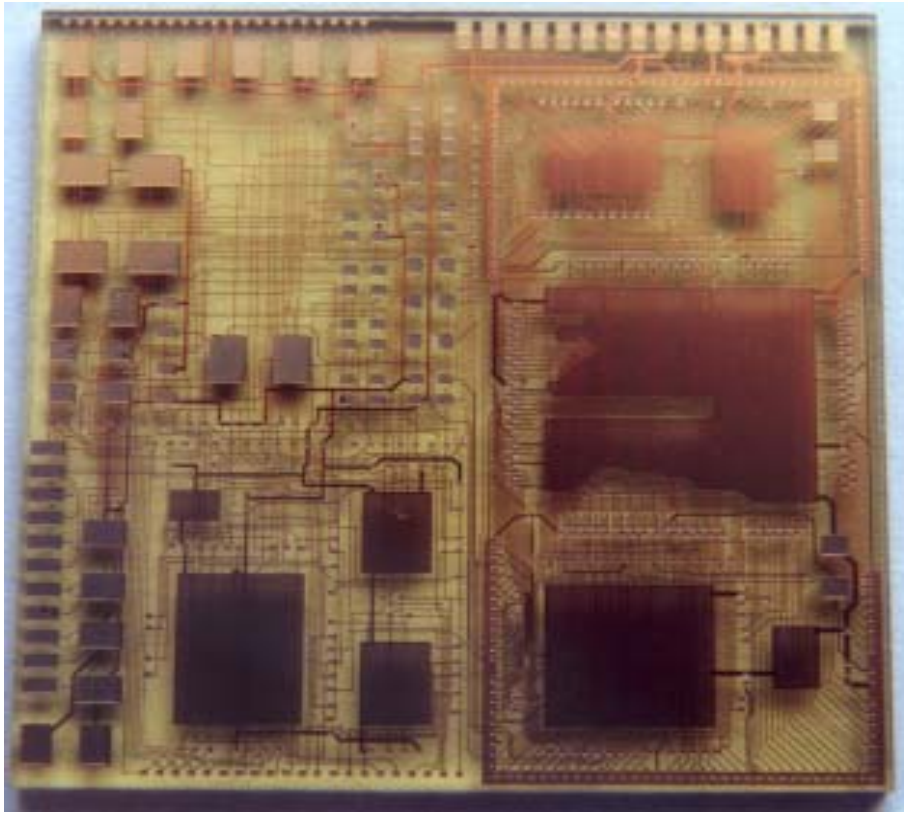
Thin film



Substrate

Thin film

Line width/pitch	> 15 / 40 µm
Via pad diameter	> 50 µm
Number of layers	2-4
Dielectric thickness	2 - 10 µm
Metal thickness	1 - 5 µm

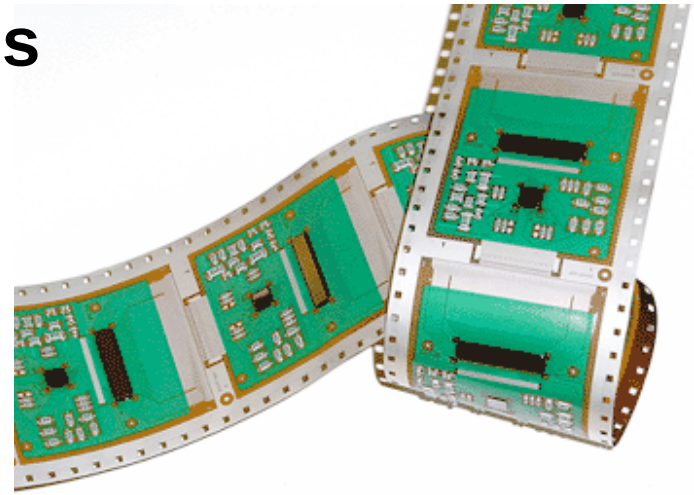


Substrates

Special Substrates

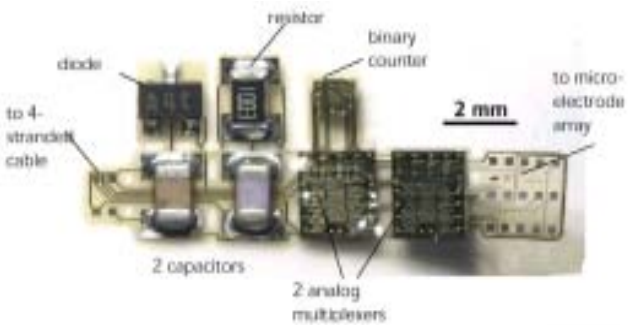
- Flex

Picture: source FhG- IZM



Picture: source SHARP

Fig. 1 High-density multi-chip SOF whose mass production technology Sharp has established



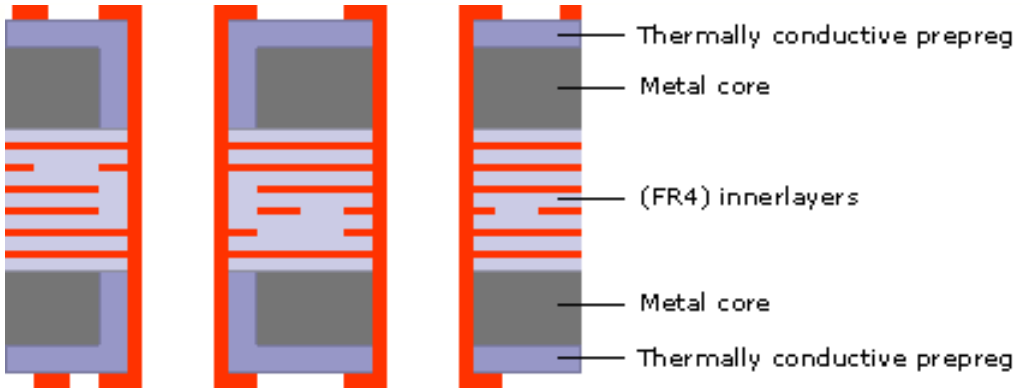
Picture: source FhG- IBMT

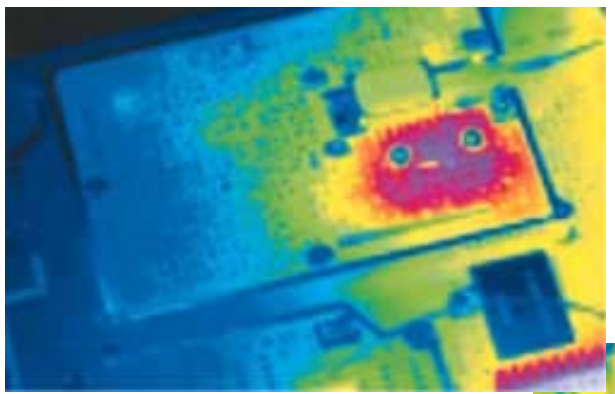
- Rigid- Flex

Thermal Management Substrates

Metall core for heat distribution

- uniform heat distribution over the whole board
- hot spots are minimized





75°

conventional FR4 build-up

Picture: source PPC Electronic

54°
Metal core build-up

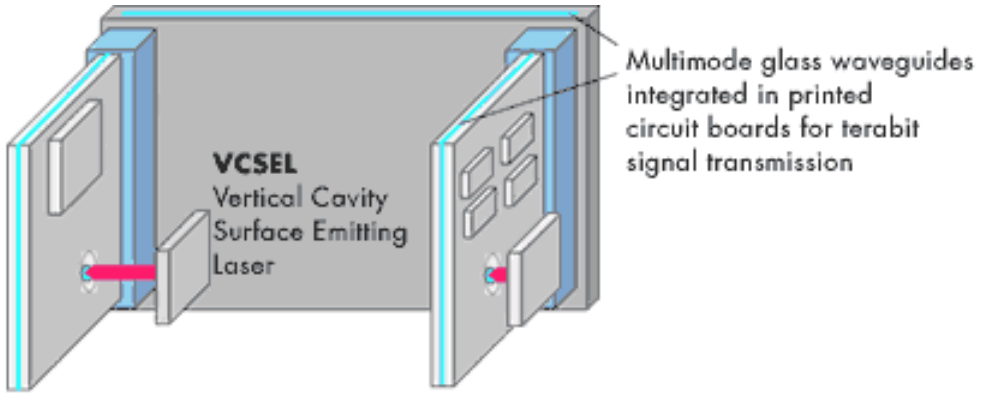
Optical Substrates

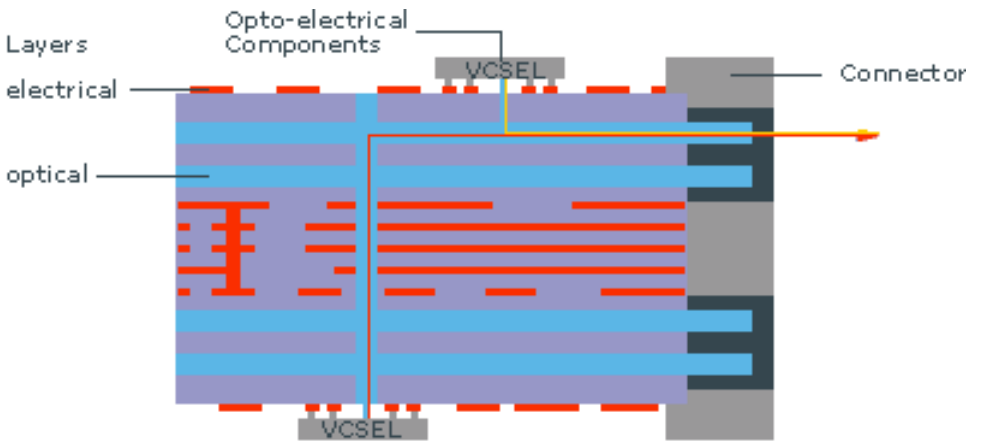
Optical planar waveguides

- thin glass
- up to 10 GHz

Passive optical elements

- mirrors, filters, couplers, splitters





Picture: source PPC Electronic

Substrates

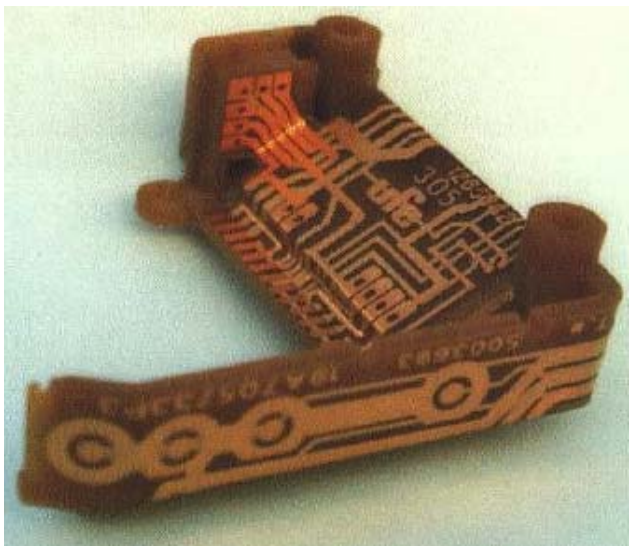
Very special types

- Electronic Textiles

Picture: source ETH Zurich

Picture: source ivf

- 3D-Moulded Interconnect Devices (3D-MID)



3D-MID moulded electronics

Why 3D-MID?

- Integration of electrical and mechanical functions
  - Printed circuit boards
  - Enclosure
  - Plug-in connectors and switches
  - Cables

3D-MID moulded electronics

Advantages

- Design freedom
  - Integration of mechanical and electronic functions
  - Miniaturization
  - Reduced seize and weight
- Rationalization
  - Reduced number of parts
  - Shorter process chains
  - Reduced material consumption
  - Higher reliability
- Environmental compability
  - Reduced variety of Materials
  - Recycling of basic materials
  - Non critical disposal

3D-MID moulded electronics

To be aware of:

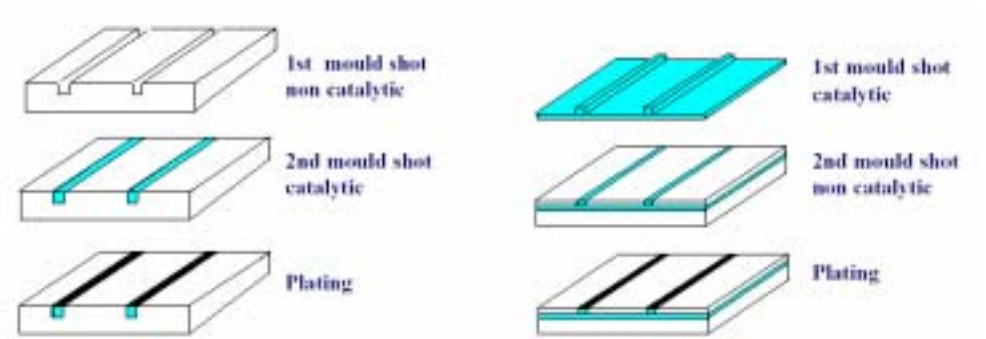
- Not suitable for assemblies with:
  - few electromechanical components
  - large printed circuitboards and more than two layers
- Full 3D production/assembly requires 6 axis control

Picture: source Räumliche Elektronische Baugruppen Erlangen

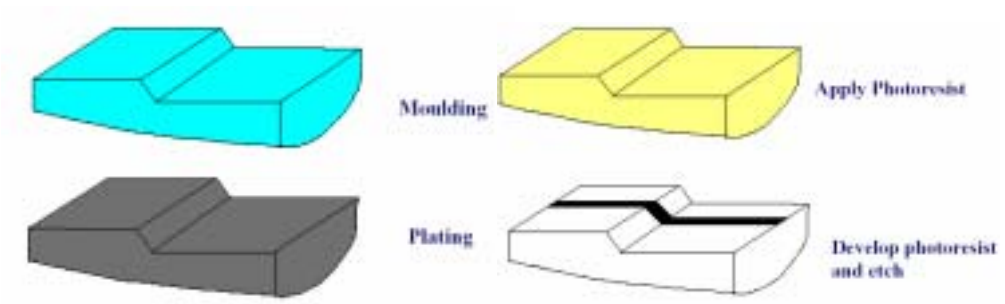
3D-MID moulded electronics

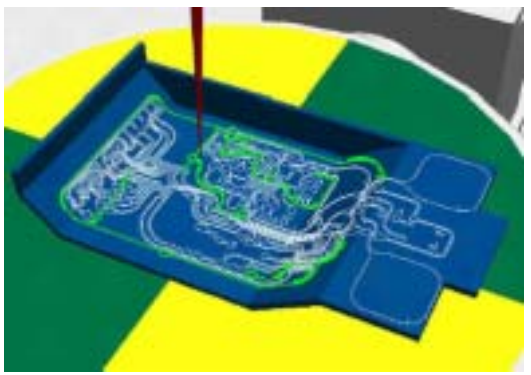
Techniques

Two step moulding



Hot embossing



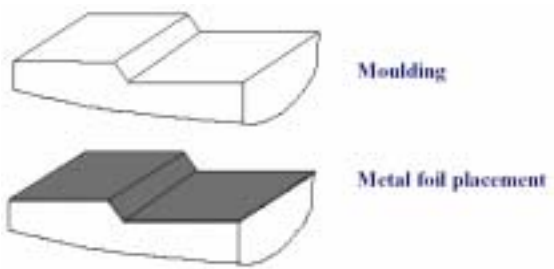


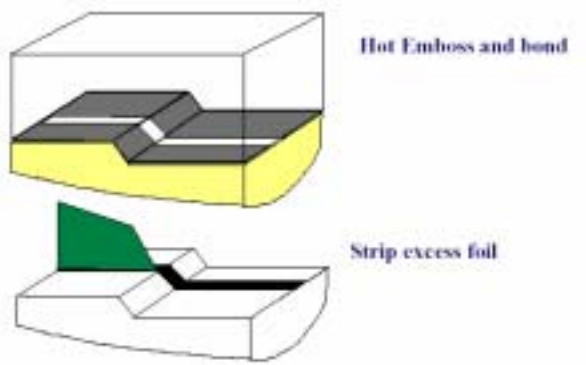
Pictures: source ivf

3D-MID moulded electronics

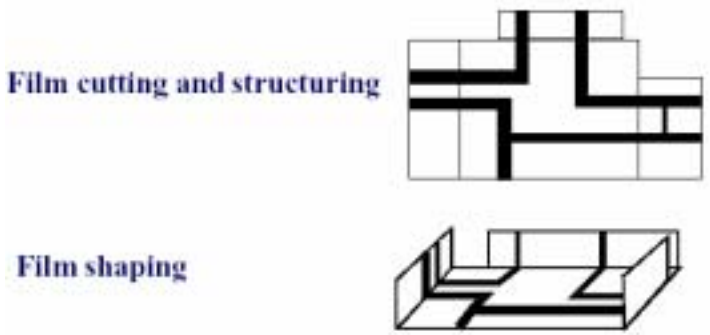
Techniques(2)

Photo-lithography





Film Over Moulding



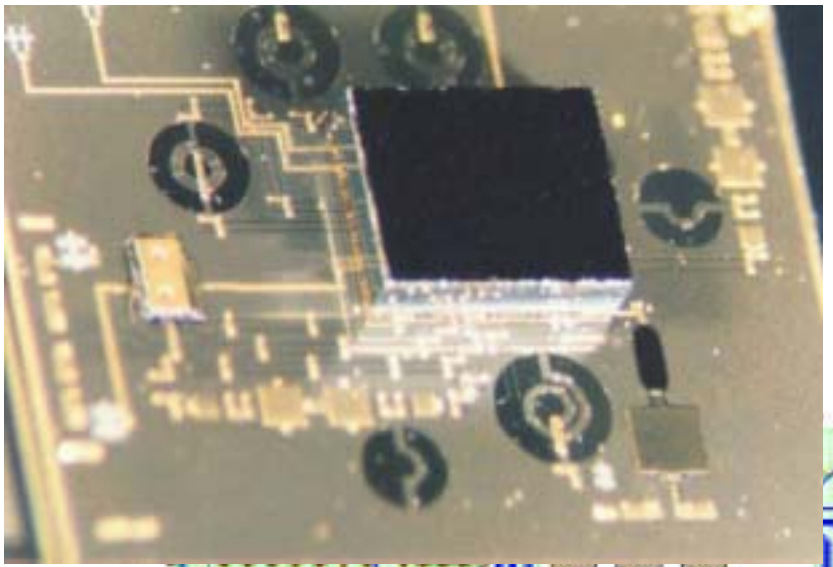
Pictures: source ivf

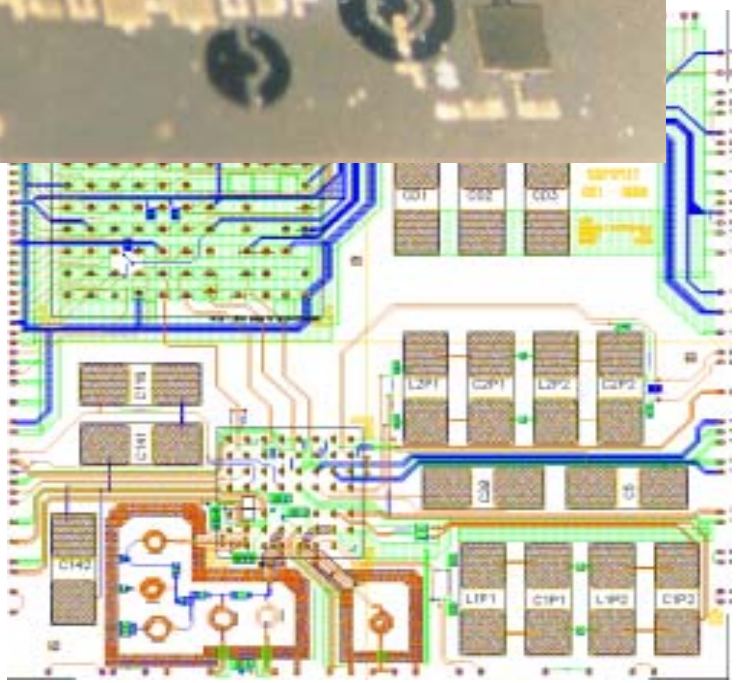
Substrate - Extras

- Integrated Passive Components
  - Resistors
  - Capacitors
  - Inductances
- Coupler
- RF Antennas
- Active Substrate

Advantages

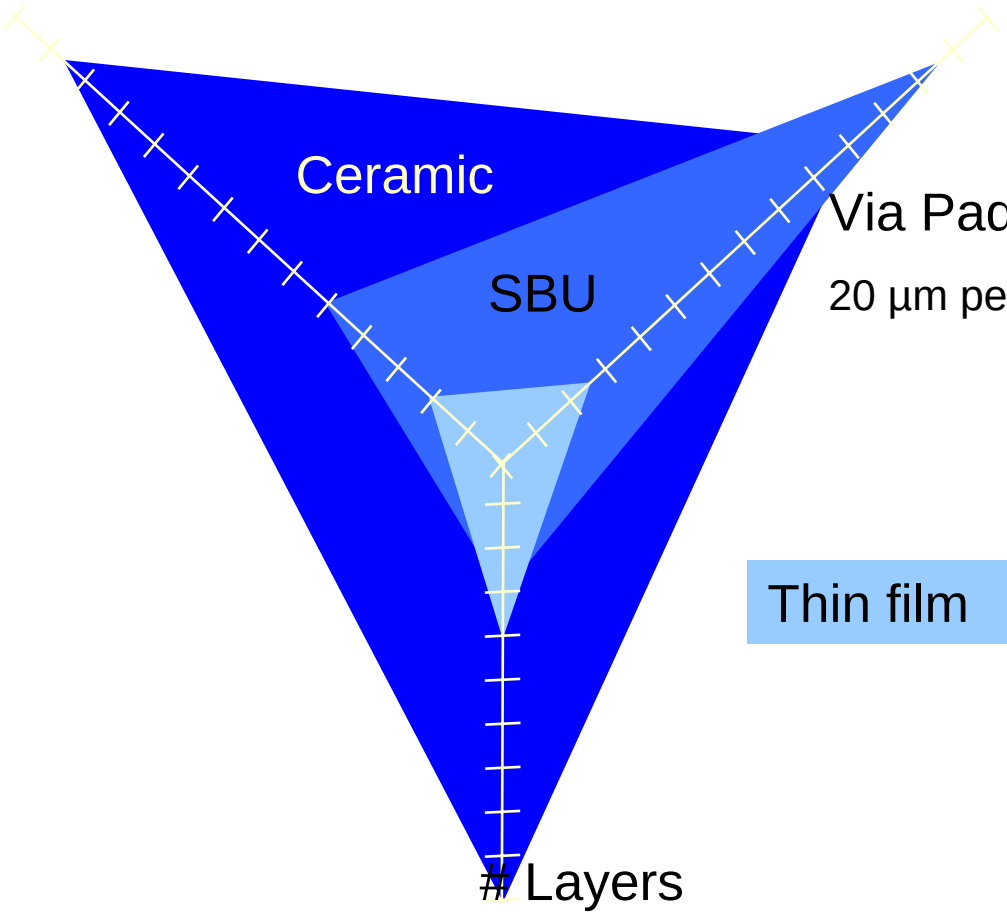
- Area reduction
- Less assembly costs
- Similar performance as SMD components





Substrate

Comparison



Line width

10 µm per unit

Via Pad diameter

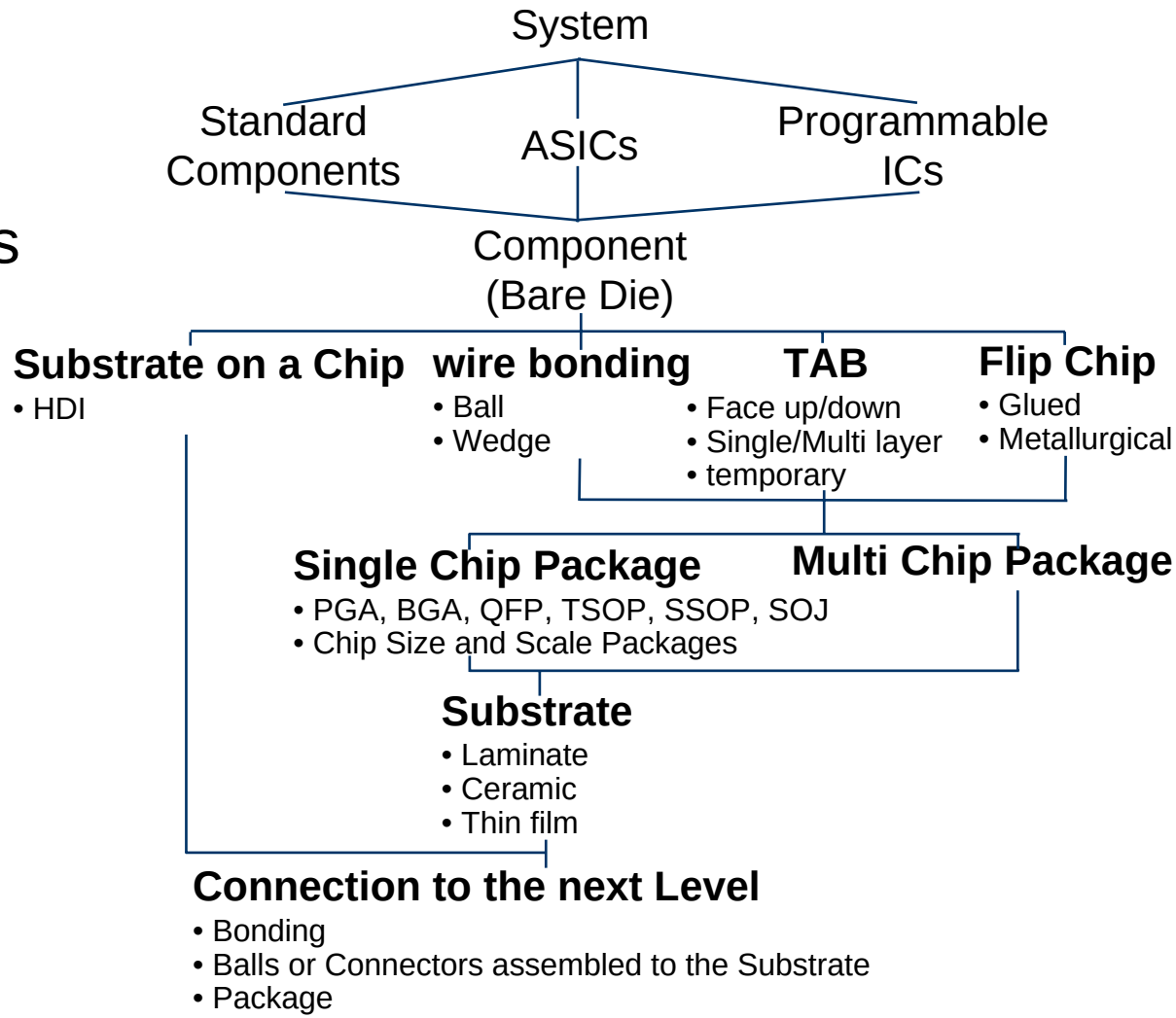
20 µm per unit

Layers

1 per unit

Summary HDP technologies

- Large Variety
- „New technologies every day“
- No general recommendation possible
- An optimal choice is absolutely necessary



Agenda

- Presentation of Art of Technology
- Motivation
- Introduction to HDP/MCM technologies
  - Definition
  - Advantages
- Technology Overview
  - Assembly/Interconnection
  - Substrates
- **Application examples**
- Typical HDP Project Flow
- Questions & Answers
- Discussion of possible customer projects

Advantages of High Density Packaging

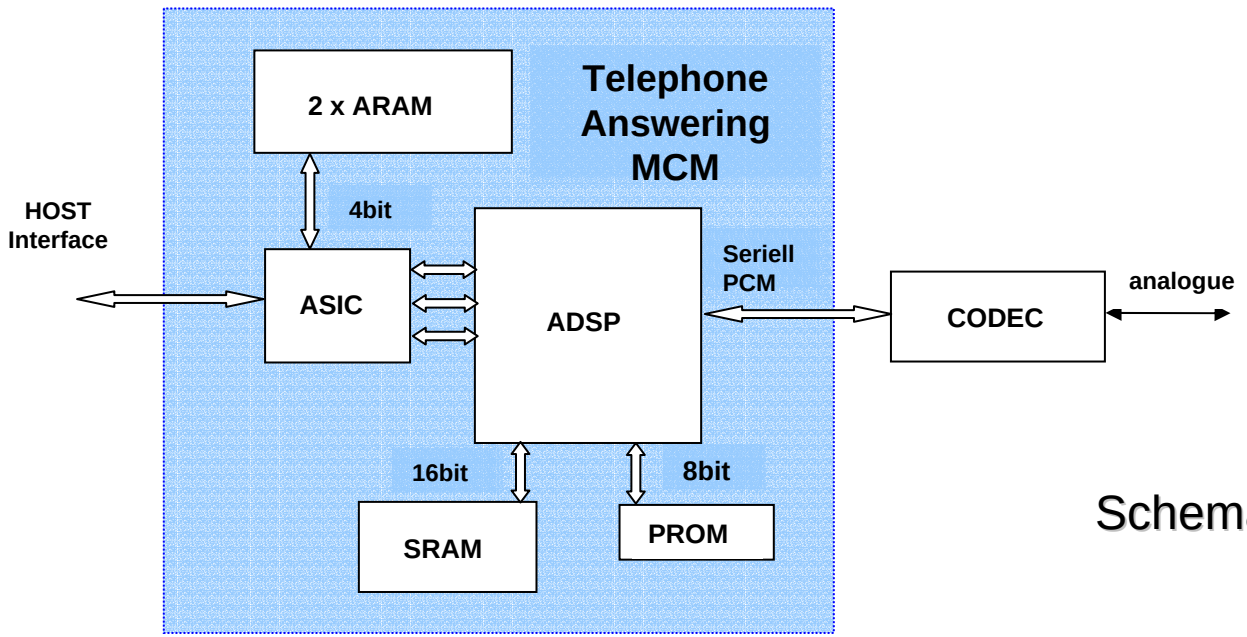
- Advantages of the HDP/MCM Technologies are ...
  - size and weight reduction
  - increased performance,reduced power consumption
  - high reliability
  - more complex systems
  - increased modularity
    - reusability
    - prevention from changes (ECO)
- … interesting for low end/high end applications

HDP Applications

- **Application Samples**
  - Telephone Answering Machine
    (Power consumption, Cost)
  - Technology Demonstrator Pentium-Modul
    (Size)
  - Commercial Modul SmartP5
    (Modularity)
  - GPS-MS1
    (Modularity, Performance)
  - Antenna Switch
    (Cost, Complexity, Performance)
  - Intelligent Power Modul (IPM)
    (Power management)

Telephone Answering Machine

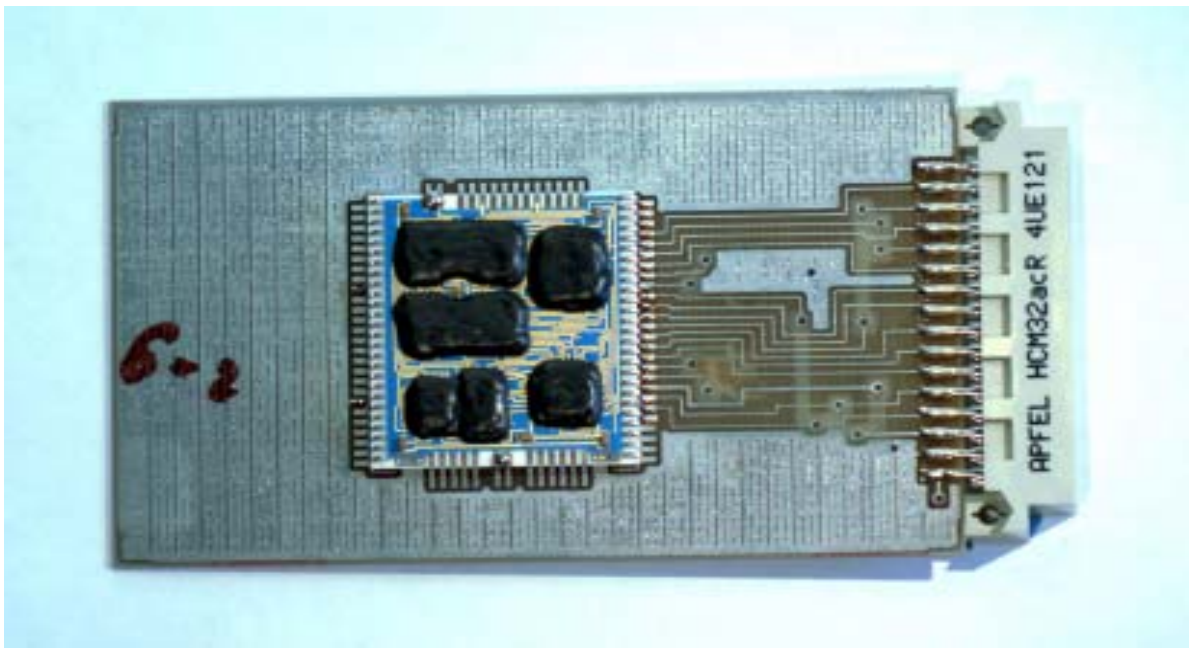
- Co-operation BWI with ASCOM, Berne
- Includes 6 Chips plus SMD Components
- Different setups



Schematic

Telephone Answering Machine (2)

1st level interconnect	Wire bond, Glob top	**Number Layers**	3	**Designrules**	180/180/400
2nd level interconnect	J-Leads soldered	**Size Substrate**	33 x 31 mm^2	**Specialities**	



Outer Board:

original size

(Module: Metallux AG)

Telephone Answering Machine (3)

- **Advantages of HDP Technologies:**
  - Size reduction down to 11% to 18% of the original size by using unhoused ICs (depending on technology)
  - Shorter distances need weaker drivers

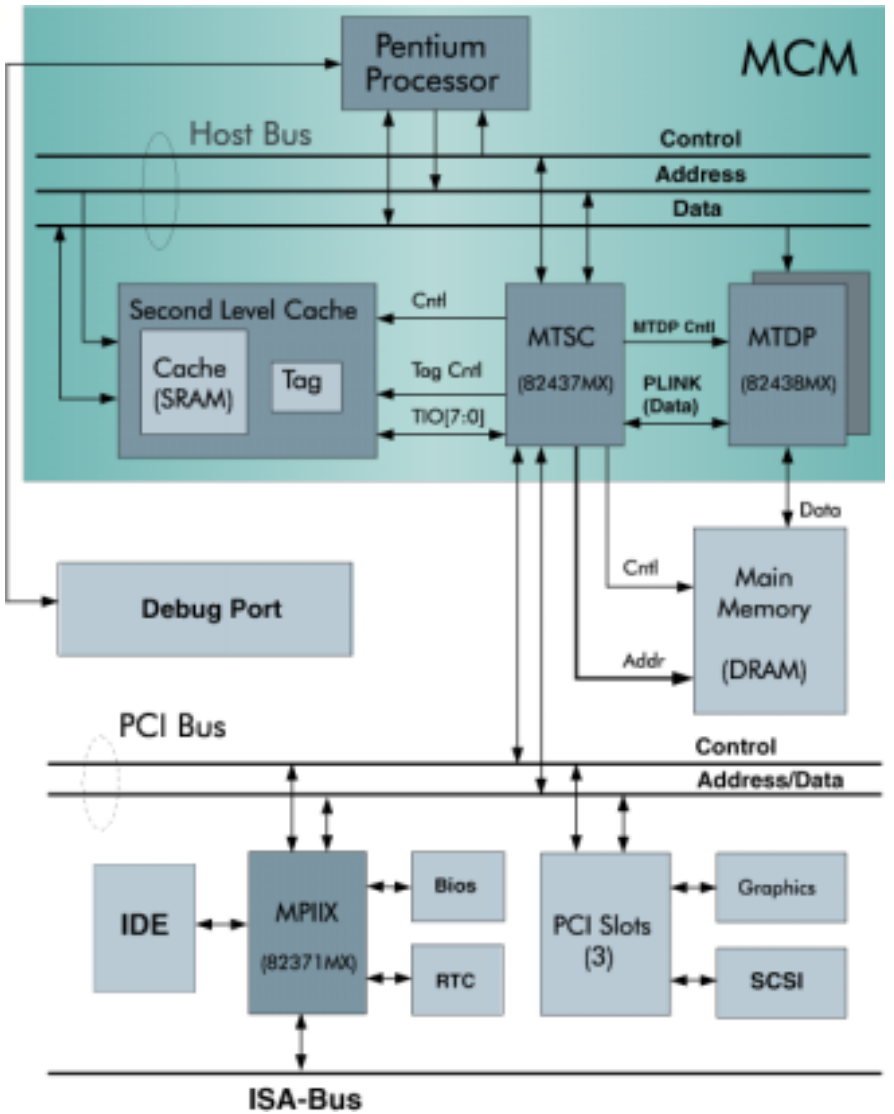
    $\Rightarrow$ Reduction of power consumption down to 66%
  - Tremendously reduced radiation

    $\Rightarrow$ no metal box required

Pentium-Module

- Technology-demonstrator
  EC Project
  Europractice

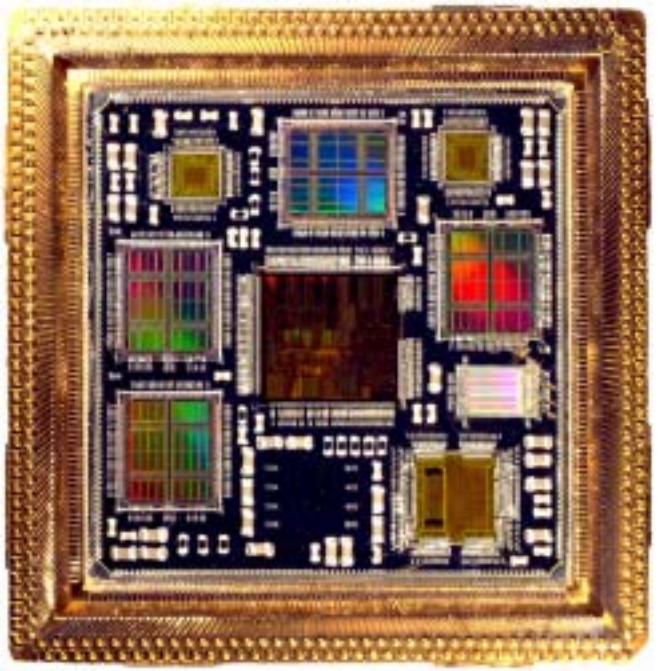
- CPU, Chip set,
  2nd level cache
  (9 Chips plus SMD components)



Pentium-Module (2)

- Thin film on Silicon a PSGA

- For over three years the smallest module, size reduction down to 25%



1st level interconnect	Wire bond, Glob top	**Number Layers**	4	**Designrules**	20/30/50
2nd level interconnect	PSGA	**Size Substrate**	32 x 32 mm^2	**Specialities**	

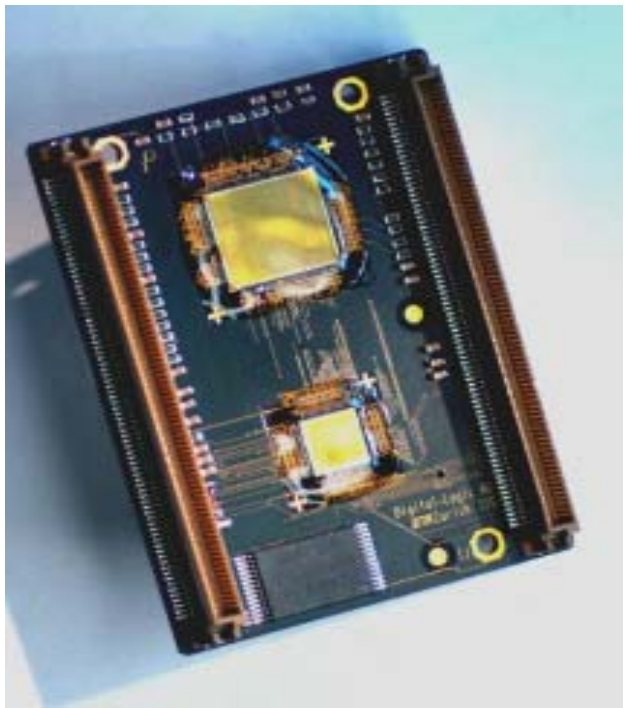
Smart P5

- Smart P5 is commercialized version of the Pentium MCM
- Designed for Digital Logic AG, Luterbach SO
- Used in a PC104 industrial computer
- Changes from the Pentium-Module:
  - Chipset in one IC
  - Power supply included

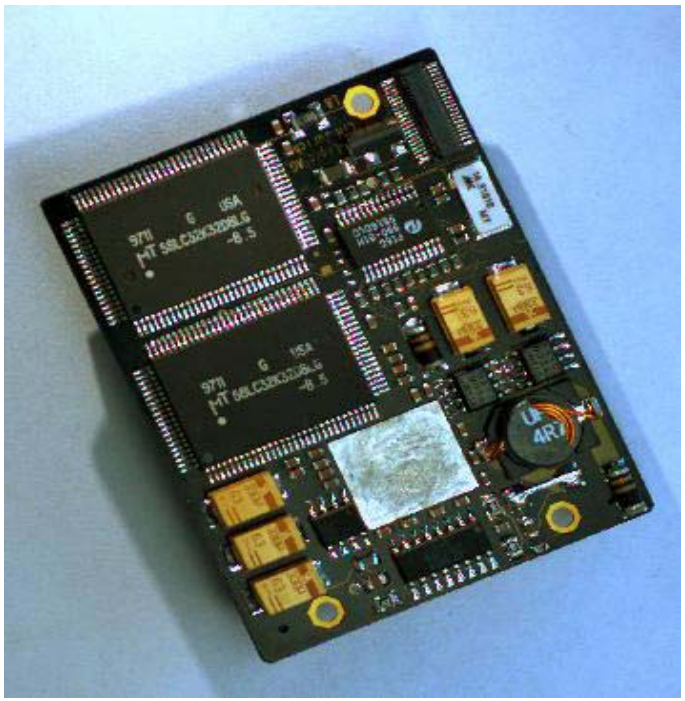
Smart P5 (2)

1st level interconnect	Wire bond, Glob top/ SMD	**Number Layers**	4 core, 2 SBU on each side	**Designrules**	50/50/200
2nd level interconnect	Connectors	**Size Substrate**	45 x 59 mm^2	**Specialities**	

Back: Bare Die



Front: SMD



Smart P5 (3)

- PCB/SBU as Substrate technology
  - Smart P5 slightly larger than Pentium-MCM, but less expensive
- **Advantages of the HDP Technologies**:
  - Size reduction
  - Increased reusability for “embedded computing” in the industrial sector
- Module has won the Innovation prize 1998, successful technology transfer ETH-Industry

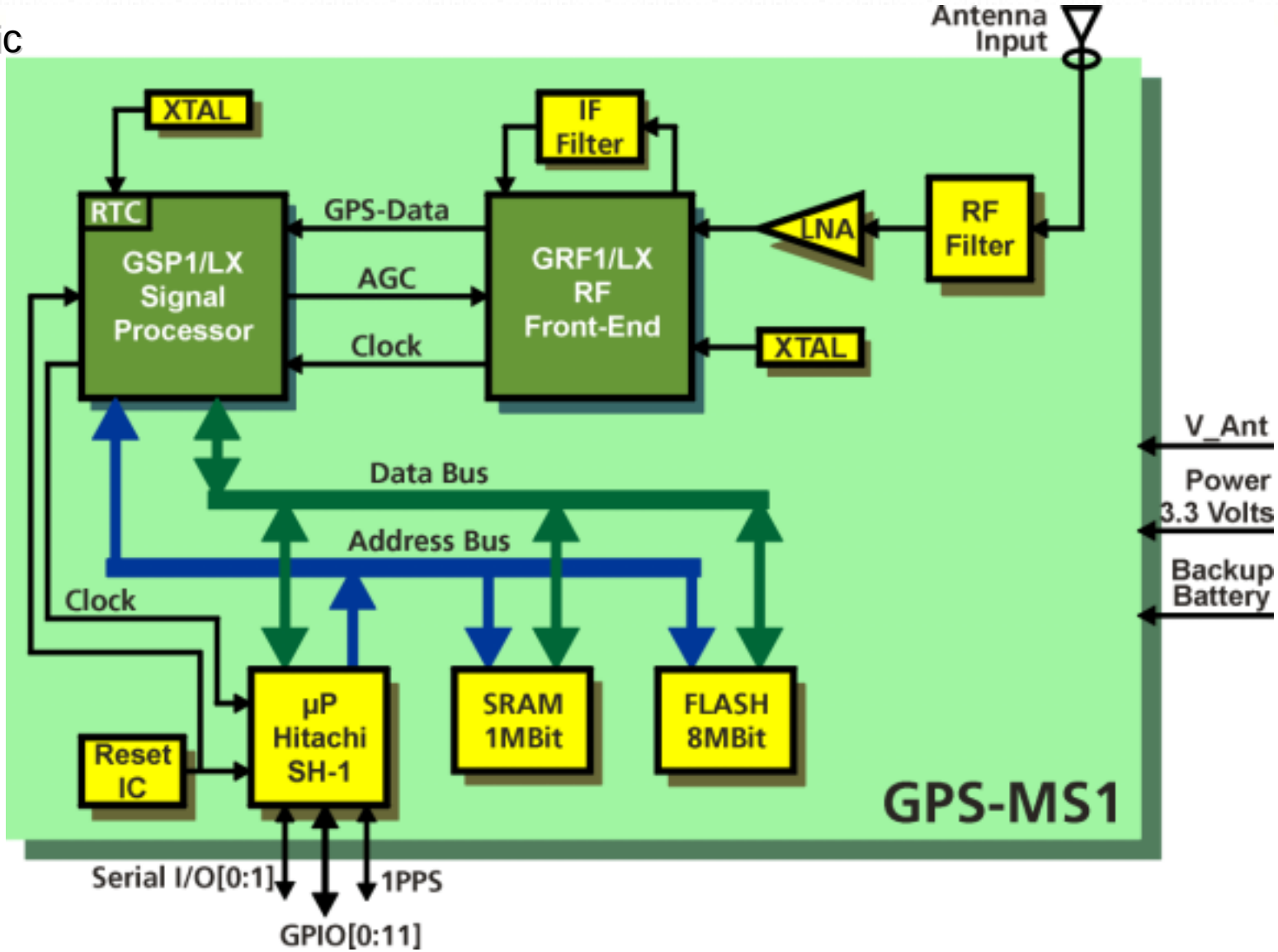
GPS-MS1

- Product of the GPS company u-blox AG
- Global Positioning Receiver
  “from the antenna to position output”

Front on Reference

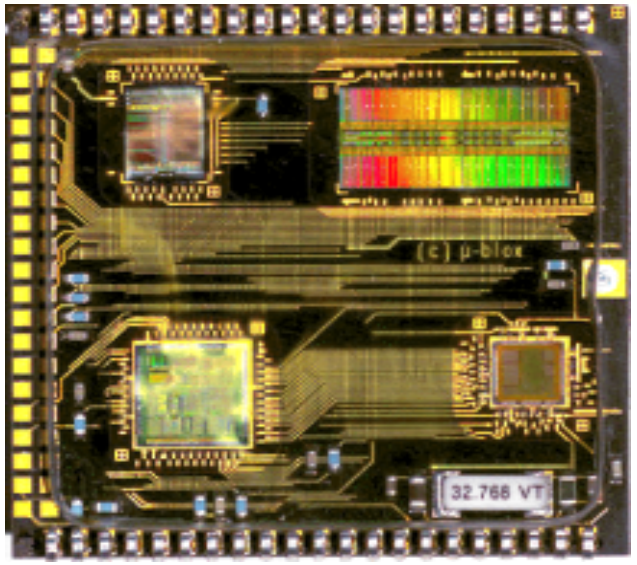
GPS-MS1 (2)

Schematic



GPS-MS1 (3)

Double-side assembled
PCB/SBU Substrate



Back with
Bare Dies

1st level interconnect	Wire bond, Glob top/ SMD	**Number Layers**	2 core, 2 SBU on each side	**Designrules**	80/80/250
2nd level interconnect	Lead soldering	**Size Substrate**	29,3 x 29,3 mm^2	**Specialities**	

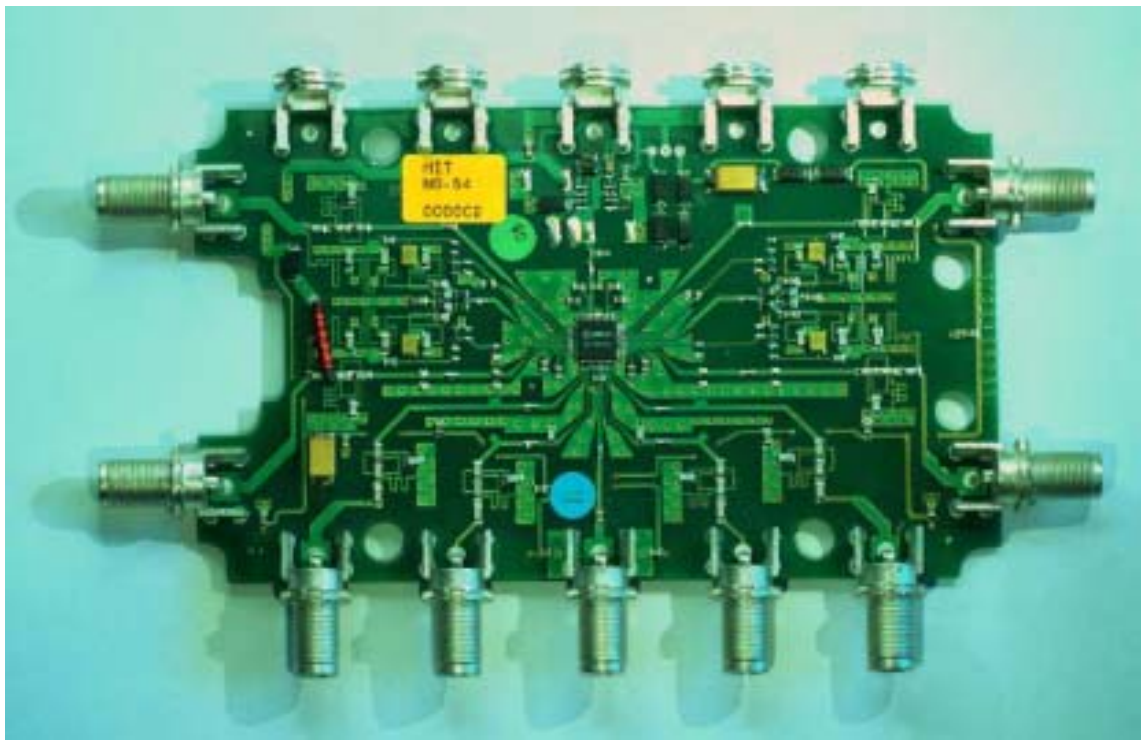
GPS-MS1 (4)

- **Advantages of HDP Technologies:**
  - Size reduction of 50-70% compared to other products
  - “added values”: free computing capacity of CPU enables new products
    (Pigeon data logger)
  - User is relieved from HF-know how
    (f_{op}=1.575GHz)
    (“it just works!”)

Antenna switch

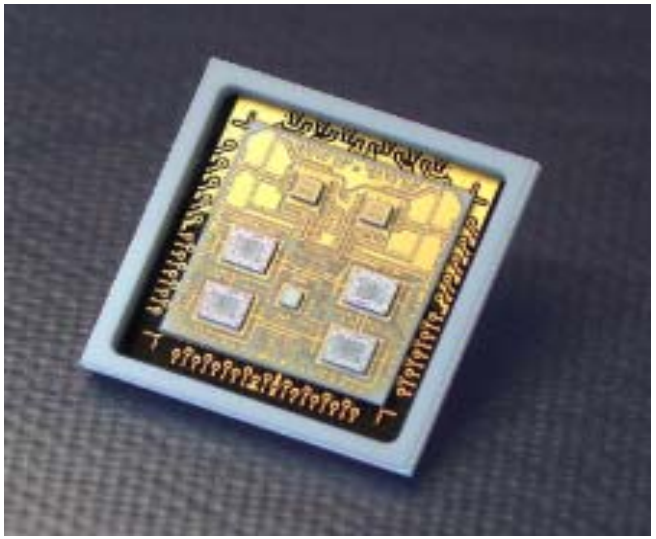
- Co-operation with Hirschmann Electronics GmbH & Co. KG, Neckartenzlingen
- Switch for satellite receiver (7 Chips)

Original PCB
with 5:4 Switch
@ 2.5GHz



Antenna switch (2)

- Thin film on Ceramic, Termination resistors and coupling capacitors integrated (right)
- COB on FR4 (next slide)

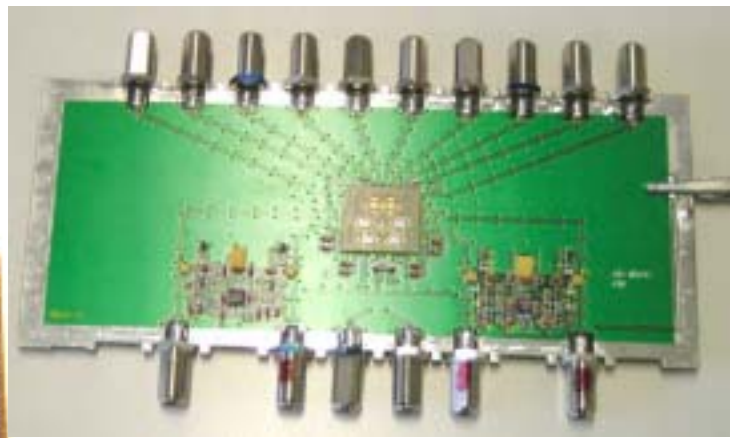


9:4 Switch Module

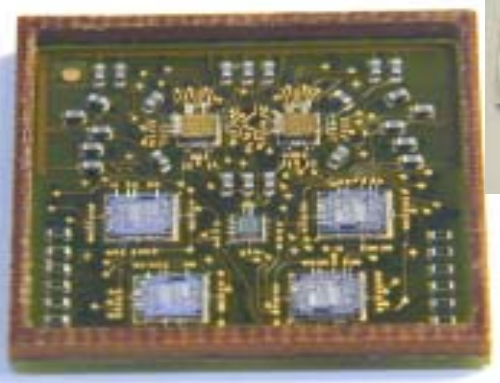
1st level interconnect	Wire bond, cap & gel	**Number Layers**	2	**Designrules**	40/60/60
2nd level interconnect	Wire bond to BGA carrier	**Size Substrate**	17 x 17 mm^2	**Specialities**	Integrated Passives

Antenna switch (3)

- **Advantages of HDP Technologies:**
  - More functionality: now 9:4 Switch (not possible before)
  - Performance-increase through shorter signal path length (f_{op}=2.5GHz)

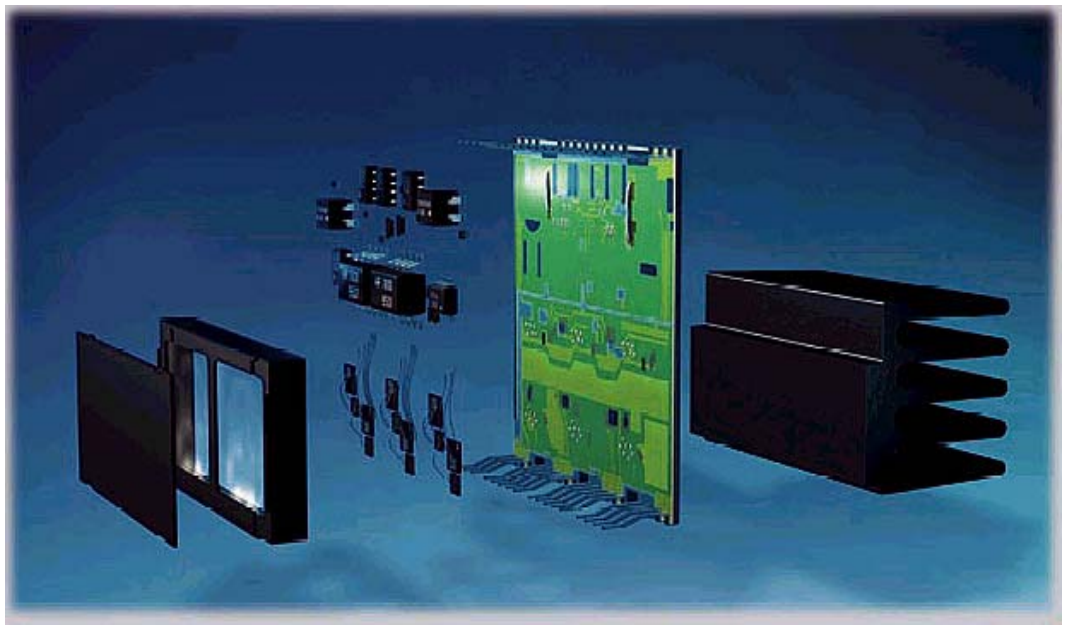


- Redesign on PCB for cost reduction



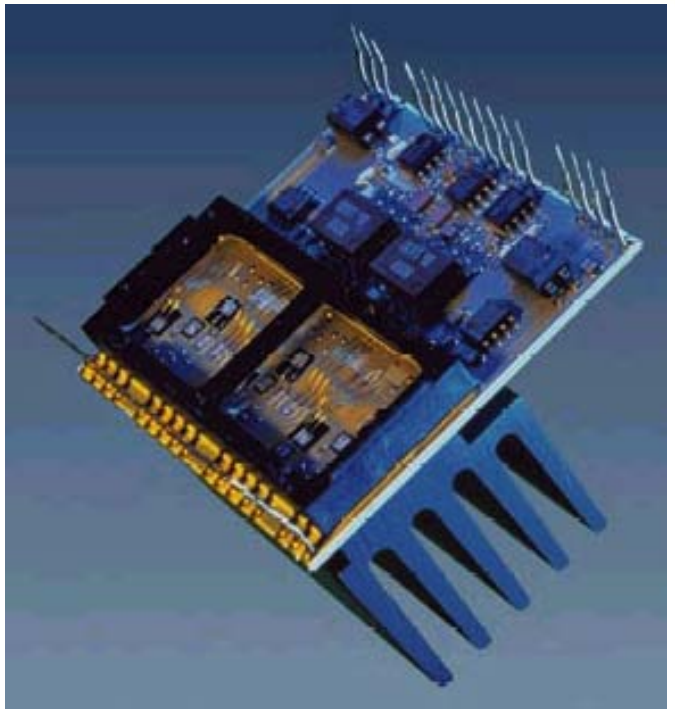
Intelligent Power Module (IPM)

- Customer specific module of **SIEMENS**
- Max 30A / 1200V
- For electrical engines up to 4 kW
- Combination of power and logic
- With cooling plate or heat sink



Intelligent Power Module (2)

- Ceramic hybrid
- Integrated shunt-resistors
- 6 IGBT's (Insulated Gate Bipolar Transistor)
- 6 FRED



1st level interconnect	Wire bond, Gel	**Number Layers**	--	**Designrules**	--
2nd level interconnect	J-Leads soldered	**Size Substrate**	51 x 49 mm^2	**Specialities**	

Intelligent Power Module (3)

- **Advantages of HDP Technologies:**
  - Very good temperature management
  - No “hot spots”

    ⇒ Increased life span of the power ICs

Summary

- Size reduction is always a benefit of using HDP.
- Further benefits depend on the product.
- A redesign is usually used to increase the functionality. For a fair cost comparison, this needs to be taken into account.

- Examples:
  - GPS**: same prize as the larger modules**
  - Antenna switch**: saves one PCB without redesigning the ASIC**

⇒ **New products can arise and new markets can be opened throughout the use of HDP**

Agenda

- Presentation of Art of Technology
- Motivation
- Introduction to HDP/MCM technologies
  - Definition
  - Advantages
- Technology Overview
  - Assembly/Interconnection
  - Substrates
- Application examples
- **Typical HDP Project Flow**
- Questions & Answers
- Discussion of possible customer projects

Project start

- We require at least one of the following inputs for a project (the more the better):
  - Idea
  - Specification
  - Block Diagram
  - Bill of material (BOM)
  - Schematics Entry
- First, a concept is elaborated by us (free of charge) and evaluated by the customer.
- Then, based on this concept and further details, a proposal for HDP/MCM design is worked out.

Project phases

- Based on specification approved by the customer, the project continues with the following steps:
  - Design/Layout
  - µC- oder FPGA-programming (if required)
  - Prototypes
  - Test
  - Pre-series
  - Test und qualification
  - Series manufacturing
- Each of the steps can be handled by AoT or by an integrated project team together with the customer.

ART OF TECHNOLOGY

Agenda

- Presentation of Art of Technology
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  - Substrates
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- Typical HDP Project Flow
- **Questions & Answers**
- **Discussion of possible customer projects**

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Thank you
for your attention!