Sept/Oct 2003

# High Density Packaging (HDP/MCM) Newsletter

**The quick and affordable way to package your electronic systems, to ensure that they are small, lightweight and robust, with protection against environmental influences.**

**Brought to you by Art of Technology, the leading European HDP/MCM miniaturization specialists.**

**When HDP/MCM makes the most sense**

- with small to medium size volumes
- when there are short development times (4 - 6 months to prototype)
- with low development costs
- modularity -when many different product variations can be built with just one module

**Expert Opinions**

**Rao Tumalla**, Chair Professor of the Georgia Institute of Technology in Microsystems Packaging, President of the IEEE-CPMT Society
"Any way you look at it, HDP/MCM is required in the future because of IC integration issues and higher I/O chips. You are limited by smallest components with finest pitch - both are difficult to achieve,beyond where we are or will be shortly. So HDP/MCM is the only way to go for those products that require either high electrical performance or smaller form factor or both."

**Ken Gilleo**, Editor of the "Area Array Packaging Handbook, Manufacturing and Assembly"
"Packaging is the bridge between fast-moving semiconductors and slow moving PWBs and is becoming more important and complex as the gap increases."

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## HDP/MCM TECHNOLOGY EVOLUTIONS

### History of Substrates

(summary of an article by Dr. Ken Gilleo in Elektronik Magazine 9/2003)

| Year | Inventor | Inventions |
|---|---|---|
| 1903/04 | Albert Parker Hanson<br><br>UK | Describes in a patent a 2-layer interconnect structure with through hole contacts. He also presented a multi-layer interconnect structure to be used in telephone switches. |
| 1904 | Thomas Edison<br><br>USA | The famous inventor was asked by the founder of Sprague Electric to provide his opinions about possibilities to replace the wire bonds, and although he never worked in this field he was able to come up with ideas that made him the inventor of the electrolytic process for the fabrication of copper sheets which is still in use today. |

| | | |
|---|---|---|
| 1913 | Arthur Berry<br>UK | Handed in a patent for the production of printed circuit board technology, using etching of metals. The required connections were printed with acid resistant Bitumen onto the metal surface which was an advantage for the punching-technique used by Hanson. Therefore he was the first to describe the etching of printed circuit boards even if it was not a photolithographic etching-process. |
| 1918 | Max Schoop<br>Switzerland | Commercialized the metal-flame-coating. This was mainly used for the production of coils. |
| 1925 | Charles Ducas<br>USA | Described the etching and electroplating of interconnect structures for radio applications …He also described other methodologies as well as multi-layer circuits. |
| 1926 | Cesar Parolini<br>France | Introduced improvements of the additive coating. He used the Edison concept and industrialized it. |
| 1933 | Franz | Printing paste was applied using different printing methods. |
| WW II | | Extremely robust electronics were required which led to the use of ceramic. In confidential projects highly robust ceramic substrates and conductive lacquers so called Cermets (ceramic/metal) were used. This also lead to the volume production of thick-film circuits. |
| 1947 | Washington D.C.<br>electronic circuit conference | Two dozen processes were consolidated into six methods: 1. printing, 2. spraying, 3. chemical deposition, 4. vacuum secretion 5. punching, 6. sprinkling |
| 1940-1960 | Paul Eisler, Austria<br>and others | Photolithography |
| Today | | Subtractive photolithography is still the dominating process used to manufacture circuit board.<br>But semi-additive processes are gaining momentum.<br>These methods require a thin conducting layer (seed metal) to start with. Then a protective lacquer is put on top. Followed by exposure to light, development and electroplating, removing the resisting material and an etching of the thin basic layer follow. The metal to be removed is minimized and the etching is no longer used to define the interconnecting structure. This is a more environmentally friendly process. The popularity of this method is also increasing because it is possible to realize very fine (<10um) lines and lines with vertical edges. Manufacturers of, free of adhesive flex substrates are now offering dielectricas with exactly the right thickness for the semi additive process. It is possible that this process will develop into the dominating one in the next few years. |
| Future | | It is possible that the existing processes are merely improved. Lasers or the nanotechnology offer possibilities but it is too early to predict what will work in large scale production.<br>Without doubt the new methodologies will be based on molecular processes. |

**From wafer to system-in package**

Summary of an article in the Elektronik Magazine 9/2003 by Tanja Braun, Karl-Friedrich Becker and Andreas Ostmann from Fraunhofer IZM in Berlin

The SMT assembly technology has since the 80s replaced ( the partially still in use) "through hole technology" because it can be automated easier.

Further increased I/O counts and the necessity to reduce size have led to the introduction of new packaging technologies such as

- BGA (Ball Grid Array)

- CSP (Chip Scale Package)
- Flip Chip
- Wafer Level Packaging

| | **Chip/Package, Pitch** | **Description and Applications** |
|---|---|---|
| BGA | >1 : 1.2<br><br>1.27 mm | Contacts are soldering balls at the bottom, which is in contrast to the usually used method,where the contacts are on the side of the chip.<br><br>A problem is the inspection after the assembly, because no visible control is possible. Therefore an x-ray inspection is being used.<br><br>But this is only necessary during the set up of the assembly process and not during production, as the process will be very stable and does not require an inspection.<br><br>BGA packages require mostly only conventional multi-layer substrates with vias. |
| CSP | 1 : 1 - 1 : 1.2<br><br>500-800 um | CSP is only size-wise different from the BGA. They are a compromise between BGAs and Flip Chips. The contacts are spread across the whole bottom and not only along the edges as with the Flip Chip.<br><br>The motivation to use CSPs is the simpler assembly, compared to Flip Chips. CSPs are used in applications such as: mobile phones, PDAs, digital video cameras. Other advantages are: easier testing because existing testing infrastrucure can be used, less stringent requirements for the substrate, no underfilling as with the Flip Chip required, a standardized connector grid makes it possible to adapt to chip layout changes without having to change the layout or assembly parameters when e.g. the chip size would be reduced (die shrink) with a new improved technology. |
| Flip Chip | 1 : 1<br><br>150-250 um | At the end of the 60s this technology was developed by IBM for mainframe applications<br><br>Dies are directly mounted or glued onto the substrate.<br><br>This happens with soldering balls that were brought onto the die beforehand (bumps).<br><br>Up until the mid 90s this technology was used for high end applications only. Improved and inexpensive bumping processes combined with inexpensive assembly processes and testing methods make this technology also interesting for other applications, Intel, AMD and Motorola use Flip Chip technology in the CPU assembly. Other high-volume applications are found in the watch modules (>200 million) and with hard disk drive read/write heads. But also smaller volume applications make use of it,such as in medical use (hearing aids, pacemakers), automobile electronics (sensors, motor controls) and the sensor industry.<br><br>Advantages are: very small form factor, higher electronic performance because of shorter signal paths, better heat distribution. Most fine pitch substrates are being used. (connector width <100um). It is required to perform an underfilling, which is adding a glue between the chip and the substrate to make the connections reliable. |
| Wafer level packaging | | A substantial cost reduction can be achieved with a complete wafer level packaging process. The advantages of Flip Chips and CSPs are combined here. The creation of interconnection structures, encapsulation and testing are all performed before separating the chips.<br><br>Additional cost reduction is possible by combining the electrical function test with the Burn-in tests of the chips all on the wafers and therefore in parallel. |

**MANUFACTURER NEWS**

**Super finelines on ceramic substrates**

A process technology is now available to producers of thick film circuitry and components,which allows them to realise conductor tracks 20 microns wide and 30 micron spaces (40 micron pitch) at high yield on ceramic. The process is based on the use of photo imageable thick film pastes which are exposed with UV light and then imaged by spin developing prior to firing. The photo imageable thick film paste includes the UV photo sensitive vehicle - so that there is no need to apply an additional photo resist layer during processing. Therefore the process sequence for producing the fine line structures is much simpler and lower cost than chemical etching processes.

Designers of high density interconnect and high frequency (GHz) circuits should consider fine line thick film as a solution especially when there are high reliability requirements.

An example is shown of a multilayer microwave test structure with high resolution photo imaged gold conductor and photo imaged dielectric on 99.6% alumina ceramic.

Further details about the technology can be found at **www.hibridas.lt**

### Moulded Interconnect Devices (MID) manufactured in series

May 2003: 2E mechatronic GmbH & Co KG, Wernau announced the deployment of the first fully automated manufacturing line for hot embossed MID components.

This line was developed and implemented within the research project AHMID. The manufacturing facility was designed for the production of different products. MID manufacturing is now already of interest for volumes starting at 50000. The technology allows the production of 3D circuits that are directly mounted onto the components.

Still under development is a manufacturing facility using lasers that allow structures smaller than 100um. This technology will be used in the future for applications within sensors and microsystems.

### Optiprint: Ni/PD/Au surface

Optiprint AG offers a universal metal coating for substrates for ultrasound and thermo sonic wire bonds: chemical Nickel / Palladium / Gold

For applications in particular where COB technologies are used, die and wire bonds are encapsulated and exposed to more stringent environmental conditions, Optiprint AG offers a finishing metallization coating for substrates, that can be wired with Aluminium and Gold bonds,and meets reliability requirements for micro systems. The substrates can be used with SMT assembly technologies.

The chemical metallization build up of 3-5 um Ni, 0.3-0.5 um Pd and 0.03 um Au offers excellent soldering and bonding parameters, with a hardness of 300-350 HV also offers cost advantages due to reduced process steps compared with electrolytic bond gold.

## EVENTS

**Event Reviews:**

### 14th European Microelectronics and Packaging Conference and Exhibition June 23rd - 25th 2003 in Friedrichshafen Germany

A summary

At first sight the conference schedule gave the impression of a mainly LTCC oriented come together. But on a closer look a lot of very interesting subjects of Microelectronics and Packaging Technologies have been presented.

In corntrary to the large amount of LTCC papers the Exhibition presented a lot of various Substrate manufacturers (many Swiss companies e.g. Varioprint AG, Reinhard Microtech AG, Dyconex AG, Cicorel SA, Optiprint AG and HighTec MC AG) but also from research at the institutes of Fraunhofer Gesellschaft over Equipment Manufacturers e.g. F&K Delvotec Bondtechnik GmbH to Assembly Houses (Microbonding SA) and System integrators (Art of Technology AG, EADS Deutschland GmbH) - The nearly 60 exhibitors at Graf-Zeppelin-House gave a wide overview of current possibilities and new in different technologies and specific manufacturing capabilities.

The Conference with 71 papers in 18 sessions and two poster sessions covered mainly the following topics:

- LTCC (Advantages, RF&Microwave, Applications)
- Materials (Under fills & Adhesives, Mat. & Processes, Lead-free & Environmental, Thick & Thin Film)
- Design & Reliability (Thermal Management, Design & Simulation, Quality & Reliability)
- Packaging (Flip Chip, CSP and Wafer Level Packaging, 3D and Stacked Packages)
- Application (Automotive, Integrated Passives, MEMS, RF & Microwave, LTCC Applications)
- Regional Packaging (European Packaging - NetPack, Asia & Pacific)

The whole three-day event with the accompanying events was a great opportunity to share know-how and news among the - mainly - European leaders in system packaging technologies thanks to the great organization of IMAPS Germany.

Further information: **http://www.EMPC2003.de**

**Upcoming Events:**

**Ineltec03**
September 2- 5, 2003
Muba-Hallen
Messeplatz, 4005 Basel, Switzerland
Ph: 0041 41 875 14 00
Fax:0041 41 875 19 86
eMail:**angela.grepper@daetwyler.ch**
**www.ineltec.ch**

**11. FED-Konferenz** "Elektronik-Design - Leiterplatten - Baugruppen 2003"
September 18- 20, 2003
Stadthalle Ludwigsburg (bei Stuttgart)
**www.fed.de**

**IMAPS Nordic Annual Conference**
IMAPS International
September 21- 24, 2003
3rd International IEEE Conference on the Nordic countries. 2003 the conference is in Helsinki University of Technology campus area.
Tutorials on September 21 and 24
Dipoli Congres Center, Espoo, Finland
**http://www.imapsnordic.org**

**MicroTech 2003**
IMAPS International
October 1 - 2, 2003
MicroTech 2003 at Stratford-upon-Avon
A two-day programme:
Day1 - Microelectronics in Medicine - The Convergence of Bioscience and Microsystems Technology.
Day2 - Polymers for Advanced Microelectronic
Structures followed by a Market Watch Panel Session.
Stratford-upon-Avon, ENGLAND, 4 The Close, Bracebridge Heath Lincoln, LN4 2PB, UK
**http://www.imaps.org.uk**

**MST'03** (Microsystems Technologies)
October 7- 8, 2003
Munich, Germany
Erik Jung **erju@izm.fhg.de**
Ph/Fax: +49-30-46403-230/161

**3rd Internat. IEEE Conference on Polymers & Adhesives in Microelectronics & Photonics**
(Polytronic 2003)
October 20- 23, 2003
Montreux, Switzerland
Bernard Courtois **polytronic2003@imag.fr**

**2003 IEEE Electrical Performance of Electronic Packaging (EPEP)**
October 27- 29, 2003
Princeton, NJ
Paul Baltes: **baltes@engr.arizona.edu**
Ph: 1-560-621-5104
Fax: 1-520-621-1443

**Productronica 2003**
11./14.11.2003
München, Germany
**www.productronica.de**

**IMAPS 2003**
IMAPS Symposium
IMAPS 36th Annual Symposium on Microelectronics. IMAPS is the largest symposium related to the microelectronics industry and the electronic packaging industry in the world.
November 16 - 20, 2003
Hynes Convention Center
Boston, MA
**http://www.imaps2003.org**